6th Joint University Students Workshop 2026
(JUSW 2026)

Nagoya Institute of Technology

Nagoya, Japan

May 13-15, 2026

6th Joint University Students Workshop (JUSW 2026)

Date: May 13 (Wed.) to 15 (Fri.), 2026
Place: Nagoya Institute of Technology, Nagoya, Japan
Bldg. #3 2nd Floor Meeting room

Topics

Power Electronics, Electrical Machines, Railway Technology and Control

Cooperation Universities

Nagoya Institute of Technology	Gyeongsang National University
Gifu University	Korea National University of Transporation
	Chungbuk National University

Schedule

May 13, 2026

・**Welcome Party (Opinion exchange for collaboration)**
18:00-21:00
Baden Baden Sakae, 6F, Gourmet Airy Building 4-5-8 Sakae, Naka-ku, Nagoya
Tel: +81- 50-3196-4667

May 14, 2026

・**Workshop**
09:30-17:30
Nagoya Institute of Technology, Nagoya, Japan
Bldg. #3 2nd Floor Meeting room
Gokiso-cho, Showa-ku, Nagoya, Aichi, 466-8555 Japan
Tel: +81-52-735-5296

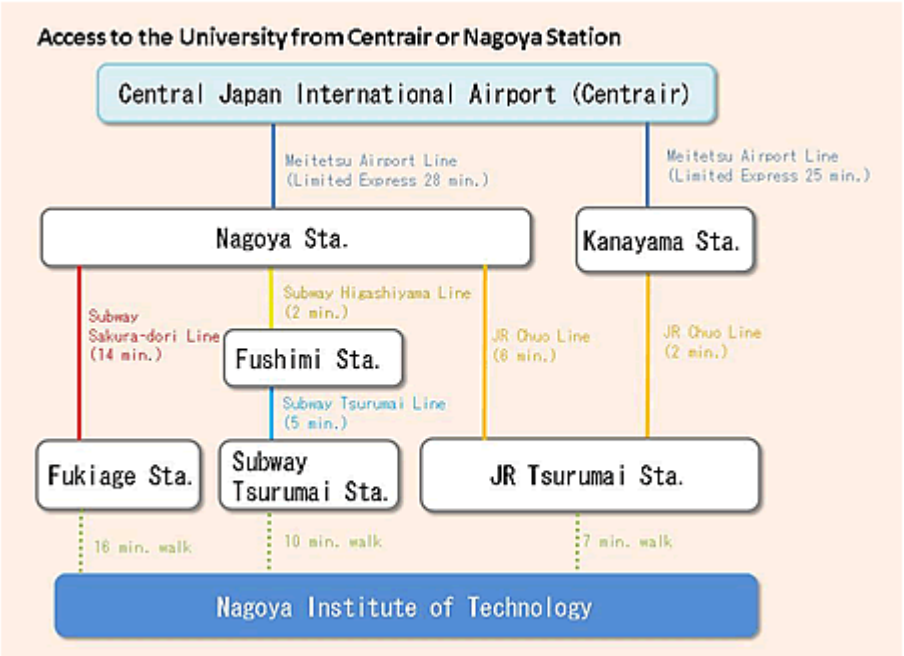
・**Dinner (Discussion about future research cooperation)**
18:30-20:30
Nagoya Beer Garden Koyoen
2-24-10 Chikusa, Chikusa-ku, Nagoya
Tel: +81- 52-741-0211

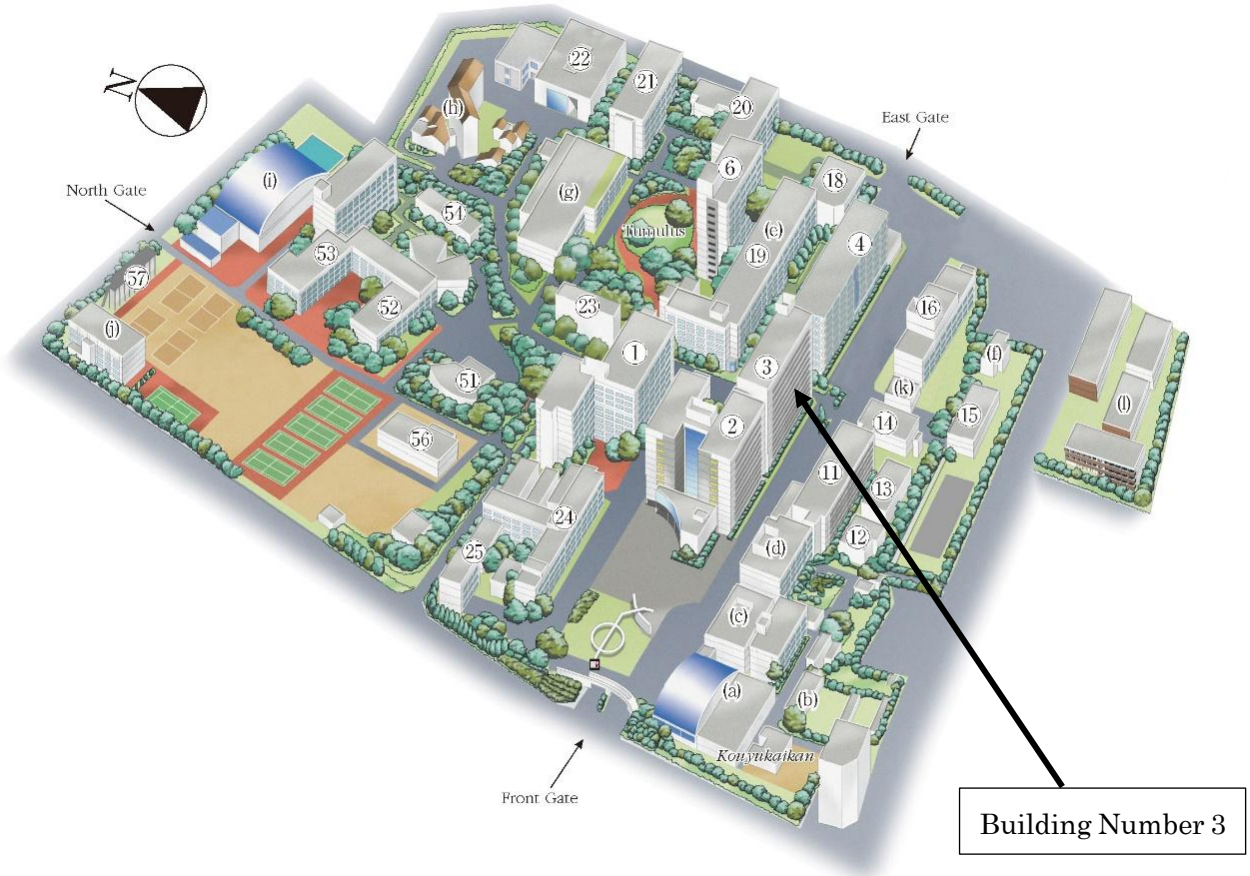
May 15, 2026

・**Lab. Tour**
10:00-12:00

Nagoya Institute of Technology, Nagoya, Japan
Gokiso-cho, Showa-ku, Nagoya, Aichi, 466-8555 Japan
Tel: +81-52-735-5441

Campas Map of Nagoya Institute of Technology





Program:

May 13, 2026

12:00-18:00 Registration

18:00-21:00 Welcome Party

May 14, 2026

Workshop

(15 min.: Presentation / 5 min.: Disscussion / 1 min.: Change the presenter)

09:30-09:39 Welcome address

Wataru Kitagawa
(Nagoya Institute of Technology)

09:39-10:00 Control Algorithm for Preventing Input Current Distortion in Totem-Pole PFC Converters

Jin Yeong Kwak*, Jeong In Lee, Tae-woong Kim
(Gyeongsang National University)

10:00-10:21 Low Power Characteristics of Three-Phase Isolated Secondary-Resonant Single-Active-Bridge DC-DC Converter Using a Y-Δ Connected Transformer

Kazuki Terazawa*, Takaharu Takeshita
(Nagoya Institute of Technology)

10:21-10:42 Coupled Inductor Design of Interleaved CF-DAB Converter for Fuel Cell

Jeong-In Lee*, Jin-Yeong Kwak, Tae-Woong Kim
(Gyeongsang National University)

10:42-11:03 A Study of Conducted Noise Overlap and Modeling in Multiple Inverters Considering Positions

Yuta Kobayashi*, Wataru Kitagawa
(Nagoya Institute of Technology)

11:03-11:24 Analysis of Gate Drive Circuit for GaN HEMT

Ji-Hyeong Kim*, Il-Hwa Jeong, Se-Kyo Chung
(Gyeongsang National University)

11:24-11:45 Cogging Torque Cancellation in Axial Gap Motors Using Multiple-Wave

Magnets with a Periodic Boundary Symmetric Arrangement

Asa Yamauchi*, Akito Mizuno, Wataru Kitagawa
(Nagoya Institute of Technology)

11:45-12:06 An Improved PWM Technique of Three-Phase MotorDrives for Common Mode Voltage Reduction

Yun-Ho Ha*, Min-Jae KIM, Se-Kyo Chung
(Gyeongsang National University)

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12:06-13:36 Lunch (90 min.)

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13:36-13:57 Development of Charging Modules for Railway Vehicle Batteries

Yeong Hun Choi*, Dong Heon Lee
(Chungbuk National University)

13:57-14:18 Design and Shape Optimization of Electromagnetic Bone Conduction Device Using Cantilever Structure

Marin Ezaka*, Wataru Kitagawa
(Nagoya Institute of Technology)

14:18-14:39 Design of a Quantile Regression Forecasting-based Robust EMS for large scale loads

Seonggyeol Kim*, Sungjoong Kim, Yubin Lee
(Chungbuk National University)

14:39-15:00 Consideration of Noise Canceling Using Electromagnetic Bone Conduction Device

Wataru Miyagoshi*, Wataru Kitagawa
(Nagoya Institute of Technology)

15:00-15:21 Development of SSCB on the Train Auxiliary Power Supply (SIV) of Urban Railway

Geonhui Hyeong*, Young-wook Kim
(Chungbuk National University)

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15:21-15:43 Break (22 min.)

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15:43-16:04 Performance Improvement of a Two-Stage Classification Algorithm in a Cloud-Based MCI Screening System Using iWakka

Sogo Ohtsu*, Kazuya Toshima, Yoshifumi Morita

(Nagoya Institute of Technology)

16:04-16:25 High-Efficiency Isolated Single-Phase Inverter Using a Phase-Shifted Full-Bridge Converter and Unfolding circuit With DQ-Repetitive Control

Eun Seop Kim*, Su Ho Park, Hag Wone Kim

(Korea National University of Transporation)

16:25-16:46 Constant DC Current Control of Unidirectional High-Frequency Isolated Medium-Voltage AC-DC Modular Matrix Converter

Kohei Budo*

(Gifu University)

16:46-17:07 Operation Analysis and Transfer Function Derivation of Three-Phase Unfolding Inverter for Renewable Energy

Su Ho Park*, Eun Seop Kim, Hag Wone Kim

(Korea National University of Transporation)

17:07-17:28 Fundamental Study on Density-Based Topology Optimization Methods in Electromagnetic Fields

Taiki Kuze*, Hideaki Nagamine, Tadashi Yamaguchi

(Gifu University)

17:28- Closing address

Hag-wone Kim

(Korea National University of Transporation)

18:30-20:30 Dinner

July 19, 2024

10:00-12:00 Lab. Tour

Control Algorithm for Preventing Input Current Distortion in Totem-Pole PFC Converters

Power Electronics and Motion Control Lab

GyeongSang National University

Presented by Jin – Yeong Kwak

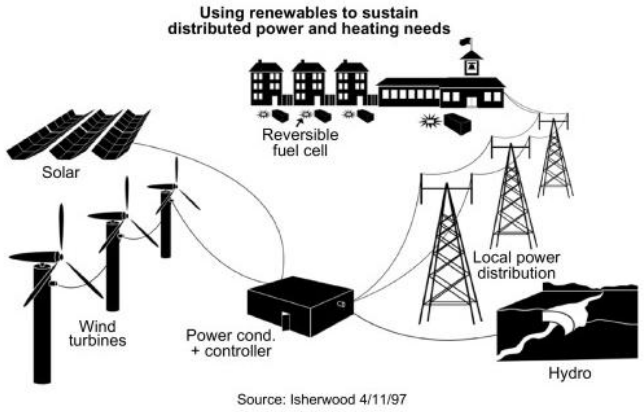
경상국립대학교
Gyeongsang National University

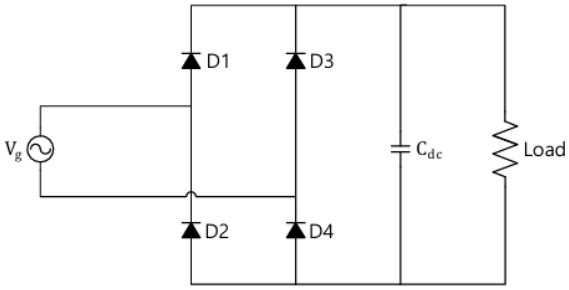
Based on GreenTech Philosophy

Introduction

Introduction

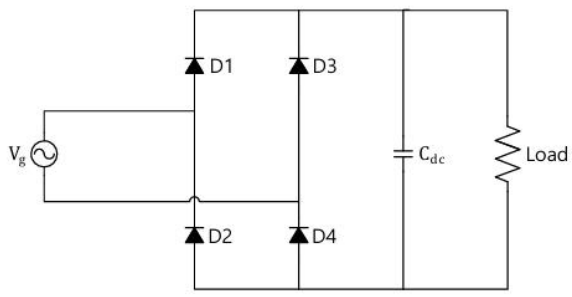
- Expansion of distributed generation systems due to the rise of renewable energy.
- Surge in demand for high-efficiency grid-connected AC/DC converters.
- Grid-connected converters must maintain a high power factor in accordance with international standards and regulations.



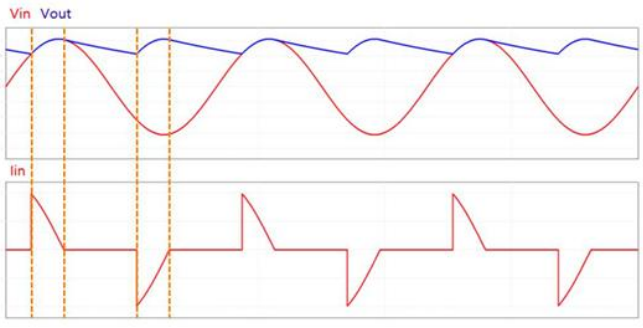


Introduction

- Diode Full-Bridge Rectifier
  - AC/DC conversion can be performed very simply.
  - Current only flows when the input voltage exceeds the output voltage, resulting in a discontinuous and distorted input current.



(a) circuit

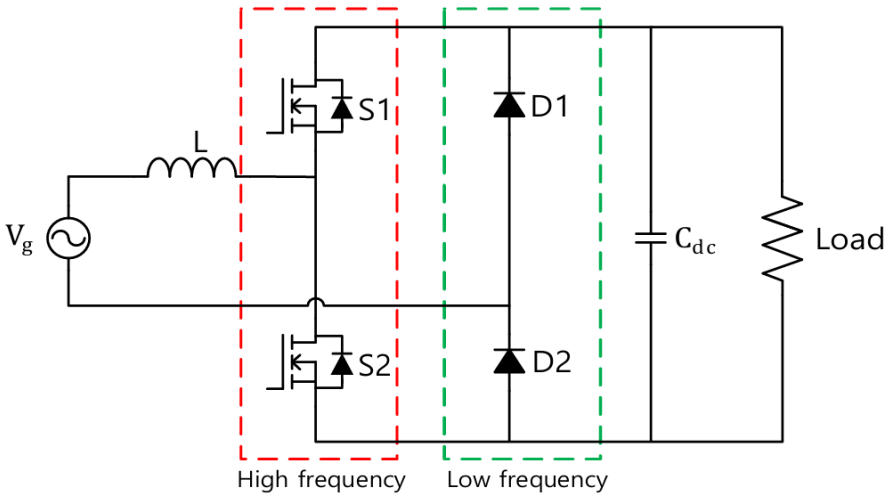


(b) input voltage/current and output voltage

Totem-Pole PFC Converter

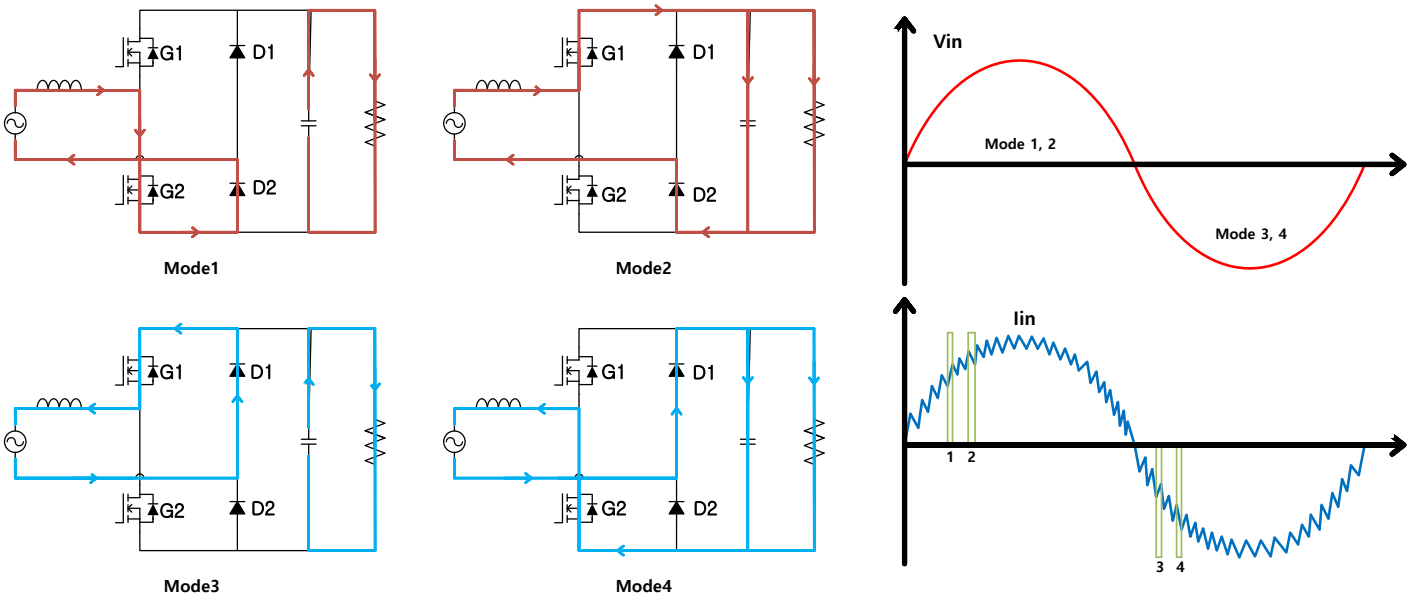
Totem-Pole PFC Converter

- Totem-Pole PFC Converter
  - Currently, the most widely adopted PFC converter, favored for its superior EMI characteristics and high efficiency.
  - S1 and S2 operate at switching frequencies many tens of times greater than the grid frequency, while the diodes switch at the grid frequency.



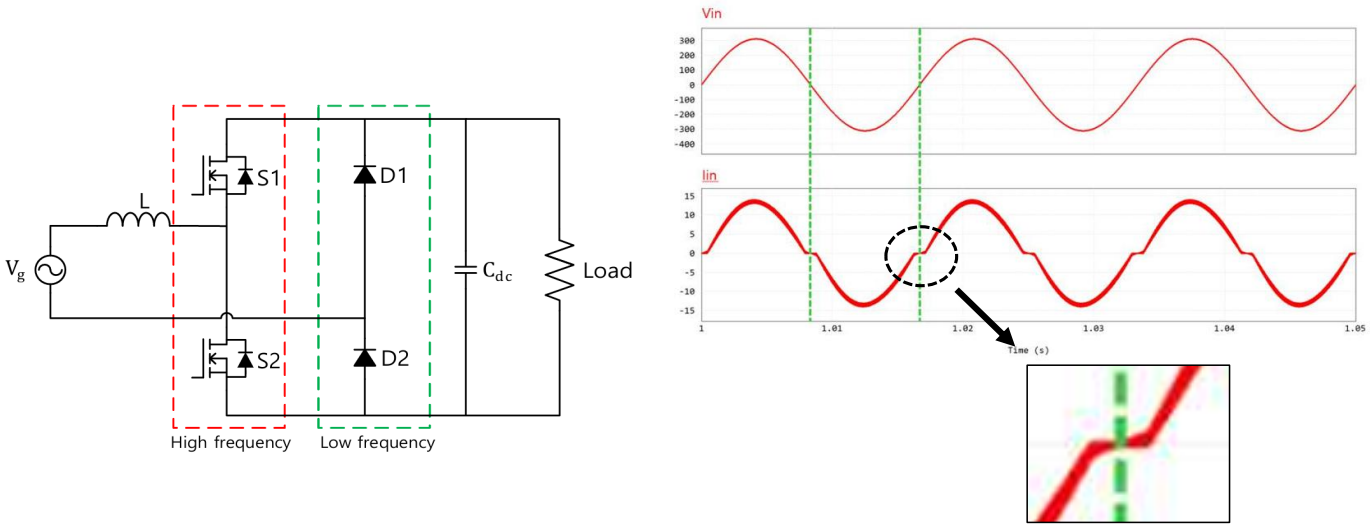
Totem-Pole PFC Converter

- Operation
  - Mode 1 and Mode 2 interleave when the voltage phase is positive.
  - Mode 3 and Mode 4 interleave when the voltage phase is negative.



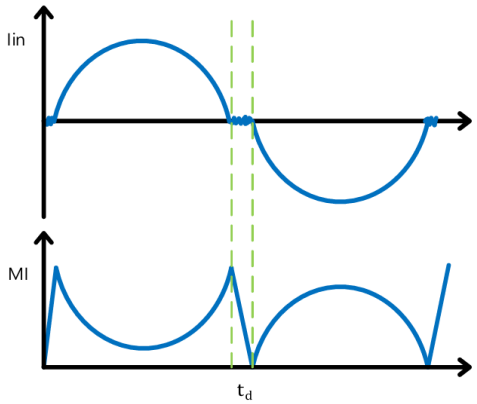
Totem-Pole PFC Converter

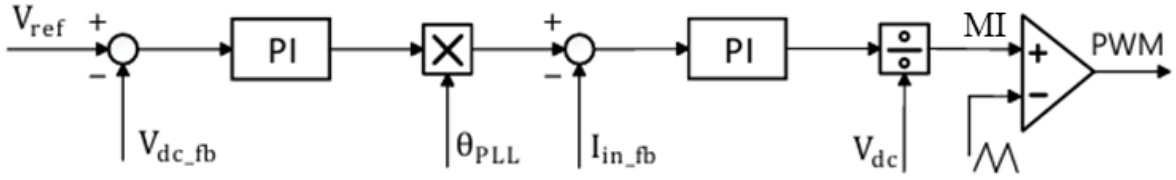
- Input Current Distortion



Totem-Pole PFC Converter

- Totem-pole PFC converters are typically controlled using a dual-loop PI voltage/current controller.
  - Unable to quickly control the rapid MI fluctuations during zero-crossing.
    - The totem-pole converter's diode conducts during the delay time(Td), causing instantaneous distortion.



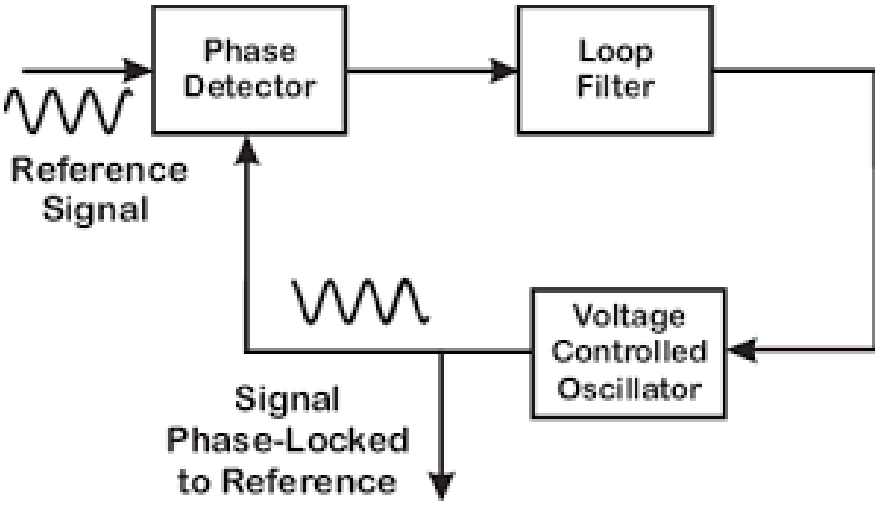


Based on GreenTech Philosophy

PLL and Proposed Control Algorithm

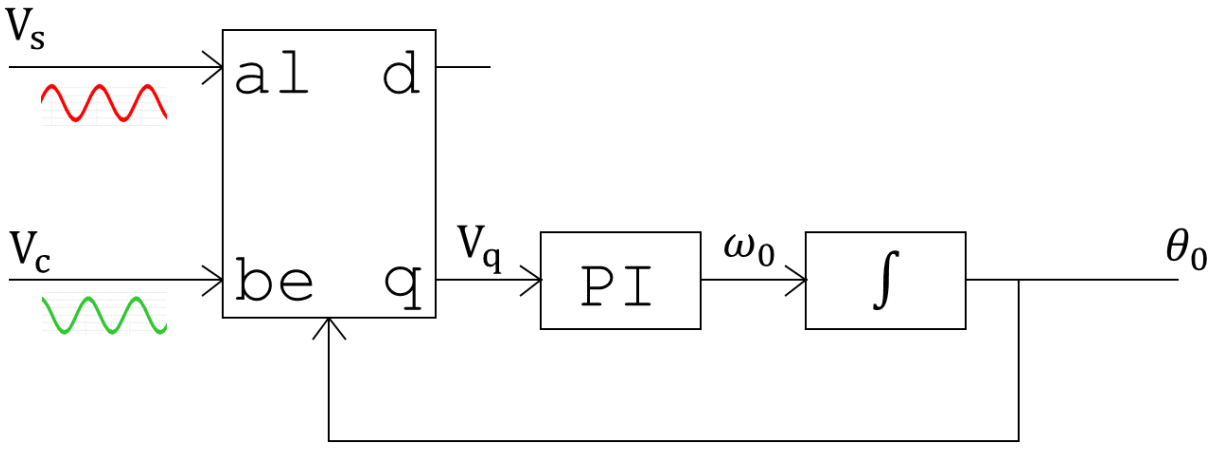
PLL

- PLL(Phase-Locked Loop)
  - A feedback loop designed to enable the output signal to track the phase and frequency of the input signal.
  - Essential for systems where phase tracking is critical, such as inverters and power factor correction converters.



SRF PLL

- SRF(Synchronous Reference Frame)-PLL
  - After converting two signals with a 90° phase difference to DC using a d-q transform, a PLL is implemented based on the q-axis output.
    - PI control reduces q-axis error.

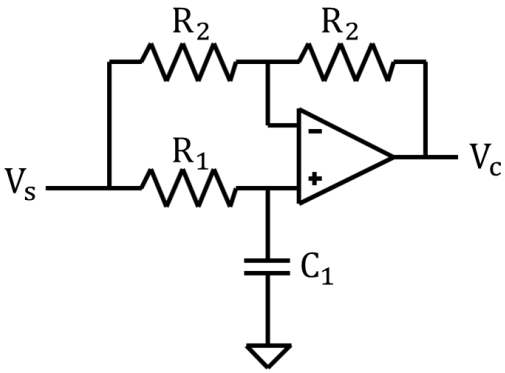


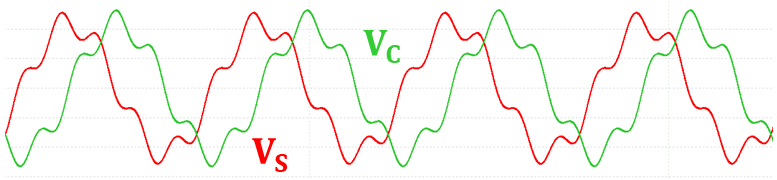
APF(All Pass Filter)

- A filter that passes all frequency band signals with a gain of 1.
  - Creates a phase difference between input and output signals depending on the combination of resistors and capacitors.

$$\phi = -2\arctan(2\pi f \cdot R_1 C_1)$$

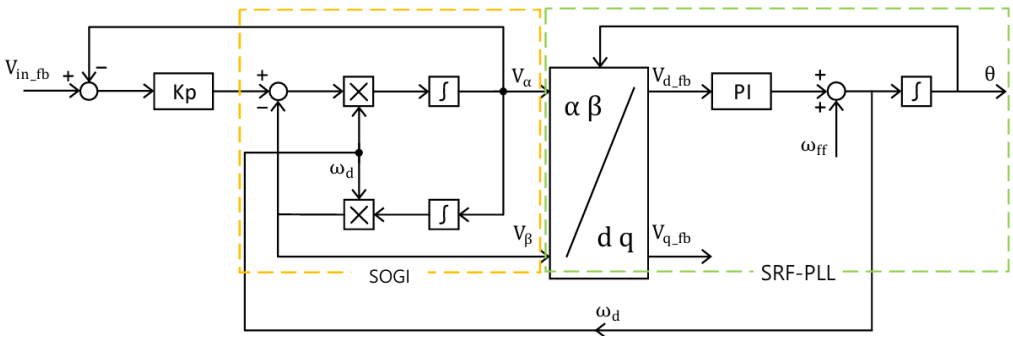
- Noise and harmonics are not filtered out and are reflected in the output.



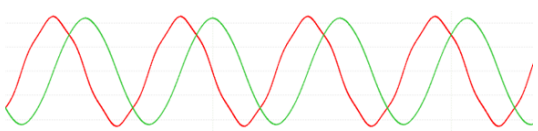


SOGI-PLL

- SOGI(second order generalized integrator) - PLL(phase locked loop)
  - Maintains stable tracking of power system phase information despite frequency fluctuations and disturbances.
  - Generates 90-degree delayed waveforms, enables dq transform & phase tracking



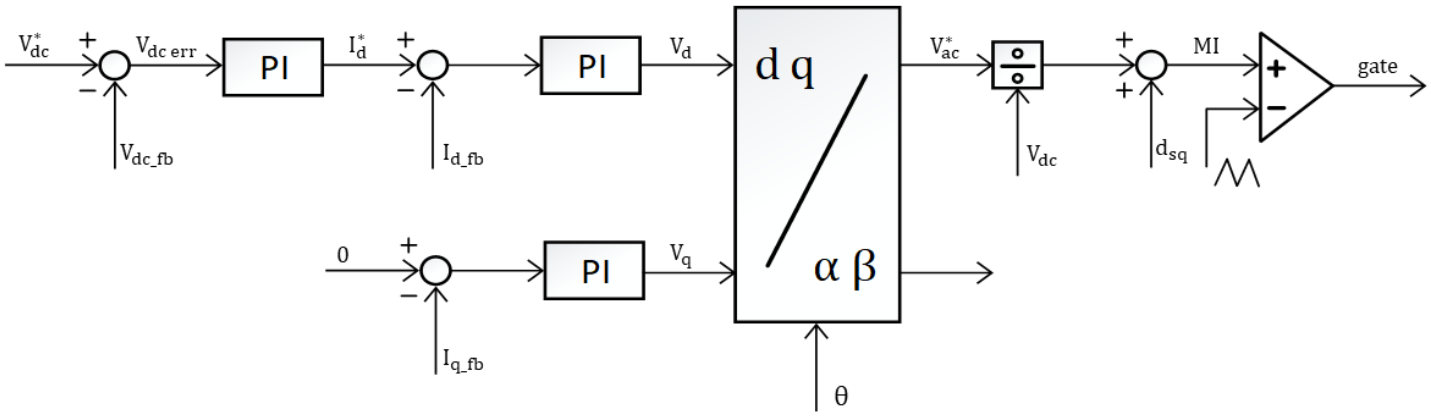
Vin



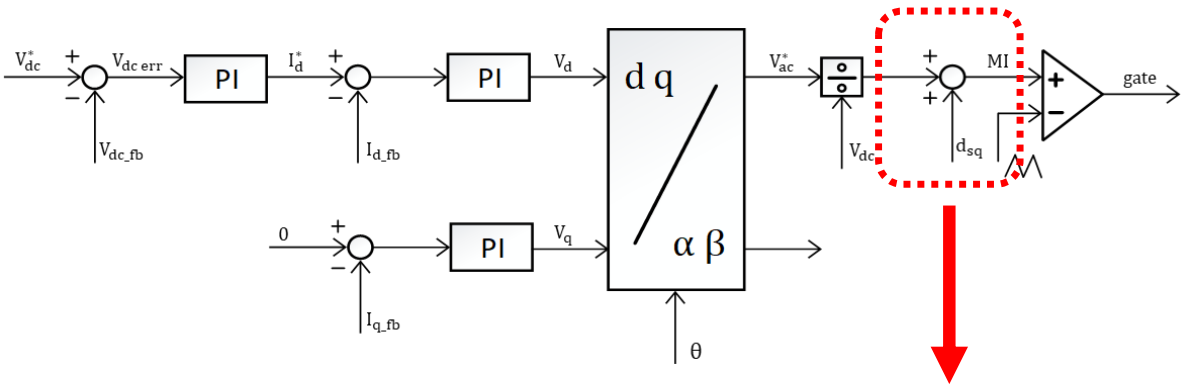
Valpha Vbeta

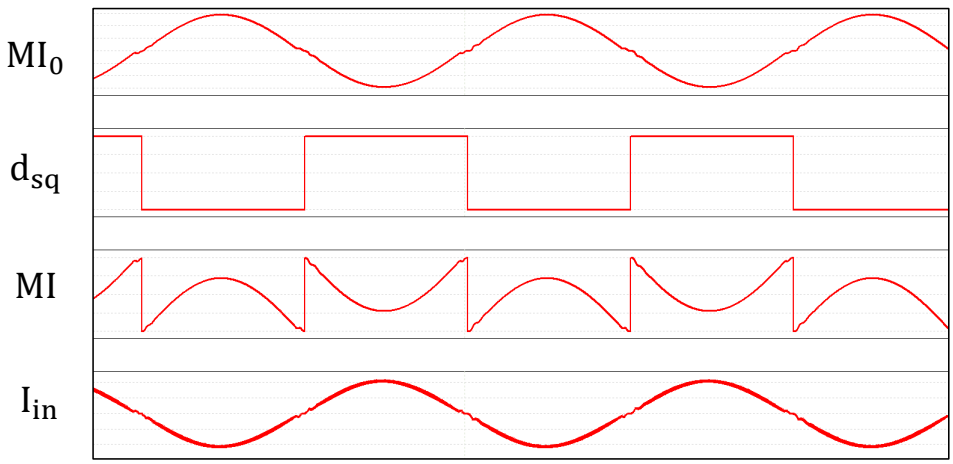
Proposed Control Algorithm

- Controls by converting AC signals to DC.
- Achieves precise control through additional compensation.
- Synchronizes input signal phase information for effective power factor correction.



Proposed Control Algorithm



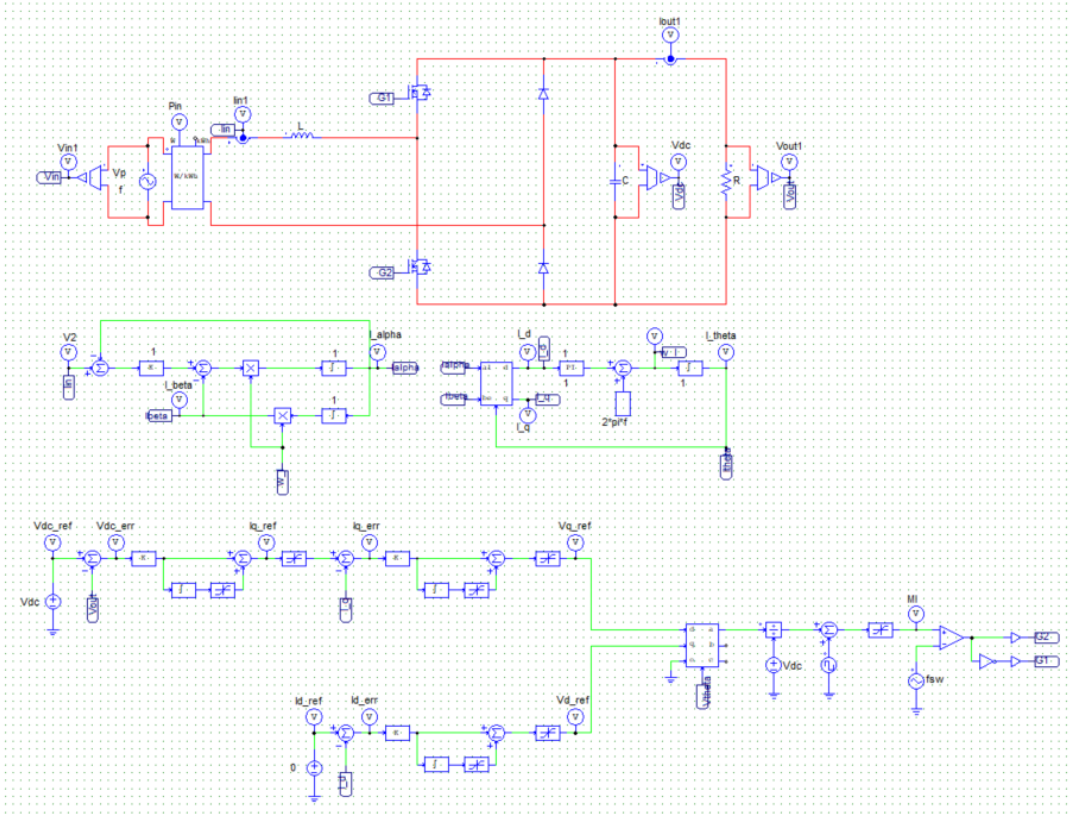


Simulation Analysis

Simulation Specifications

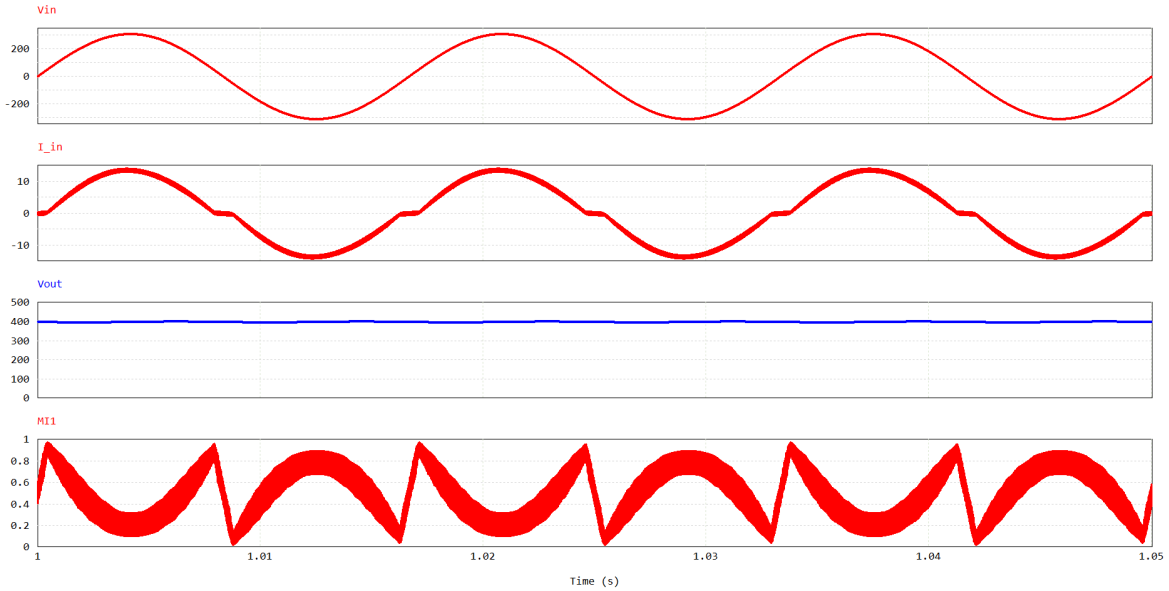
parameter		value	parameter		value
Power	P_{in}	2kW	Input Inductor	Lin	1500uH
Input V	V_g	220Vrms	I ripple	ΔI	10%
Grid f	f_g	60Hz	V ripple	ΔV	2%
Output V	V_{dc}	400Vdc	Output C	C_o	5%
Load	R_{Load}	80Ω	Switching f	f_{sw}	50kHz

Simulation Configuration



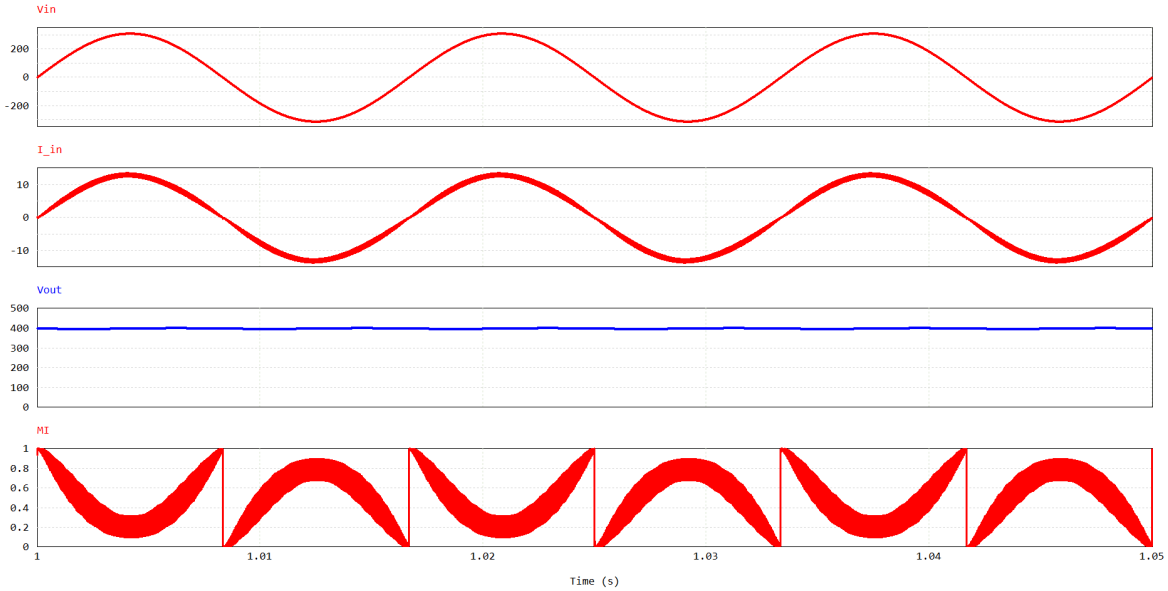
Simulation Result

- Before compensation



Simulation Result

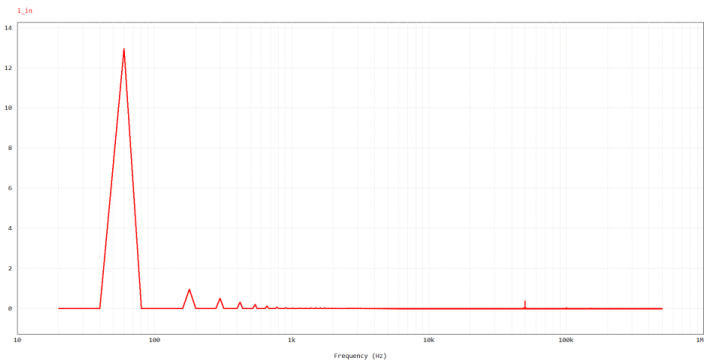
- After compensation



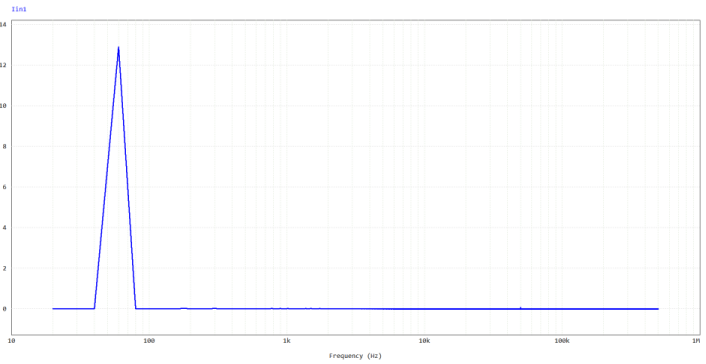
FFT Analysis

- $\mathrm{THD} = \frac{\sqrt{\sum I^2/h}}{\mathrm{I}_1}$
  - h = Harmonic Order

h	Before compensation	After compensation
3	4.244%	1.394%
5	1.729%	0.076%
7	0.938%	0.243%
9	0.545%	0.081%
11	0.319%	0.126%
THD	7.757%	1.92%



기존 PI제어



dq 좌표변환 기반 PI제어

Conclusions

Conclusions

- Summary
  - The control algorithm proposed in this study was validated through PSIM simulations, demonstrating its ability to mitigate current distortion and stably regulate the output of a totem-pole PFC converter.

- Future works
  - To experimentally validate the proposed algorithm, we are currently fabricating a 1kW SiC-based prototype system board. Experiments are scheduled to commence upon its completion.

Thank you for your attentions

Questions & Answers

Power Electronics System
Power Conversion System / Electric Motor Control
Smart Energy Control System / Green Energy System

Low Power Characteristics of Three-Phase Isolated Secondary-Resonant Single-Active-Bridge DC-DC Converter Using a Y-Δ Connected Transformer

Kazuki Terazawa*, Wataru Kitagawa, Takaharu Takeshita

Nagoya Institute of Technology, Japan

May 14, 2026

Research Background and Purpose

Background

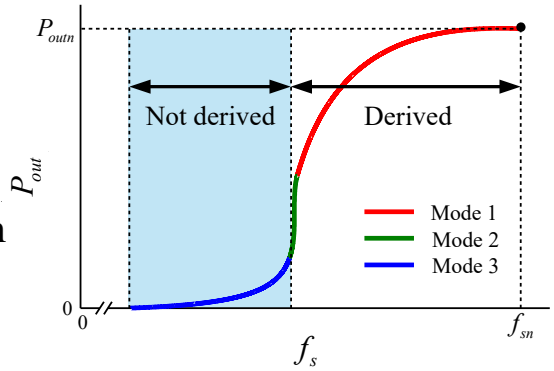
Environmental issues : Achieving carbon neutrality
→Quick chargers for EVs and DC power distribution system

Three-Phase Isolated Secondary-Resonant Single-Active-Bridge DC-DC Converter Using a Y-Δ Connected Transformer
・compact ・high-efficiency ・high-power

Derived { Mode 1 : representing the range around the rated power
Mode 2 : output power rapidly changes

Not derived { Mode 3 : representing low power operation

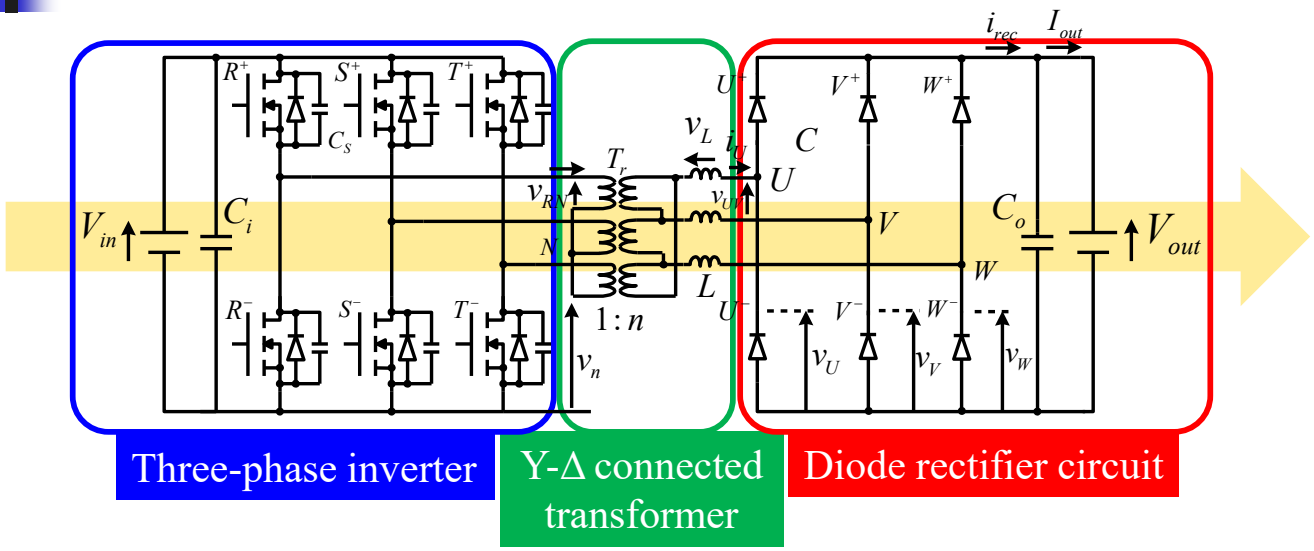
Theory is necessary for proper circuit design



➢ **Purpose**

Derivation of Low-Power Characteristics for Zero Output Power

Conventional circuit

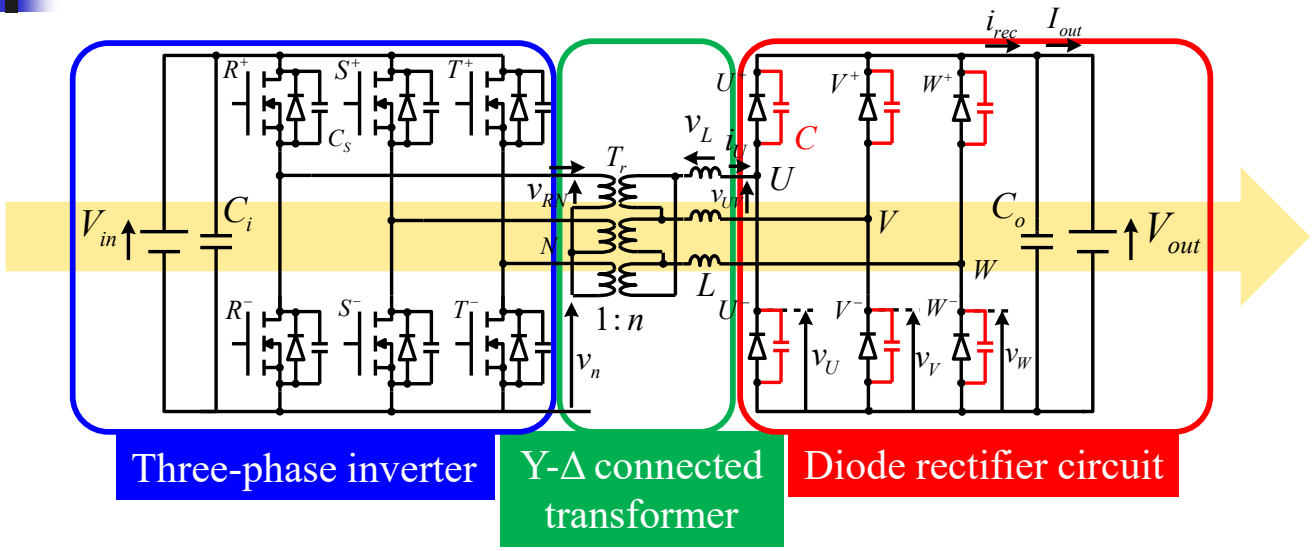


Single-Active-Bridge (SAB) DC-DC converter

◎
- The secondary side consists of passive components
  → Unidirectional power transmission ・ Simple circuit configuration
- Loss reduction by soft switching

△
- Increased transformer capacity → Larger circuit size
- Higher input voltage than load voltage required → High-voltage devices

Proposed Circuit



Secondary-Resonant Single-Active-Bridge (SR-SAB) DC-DC Converter

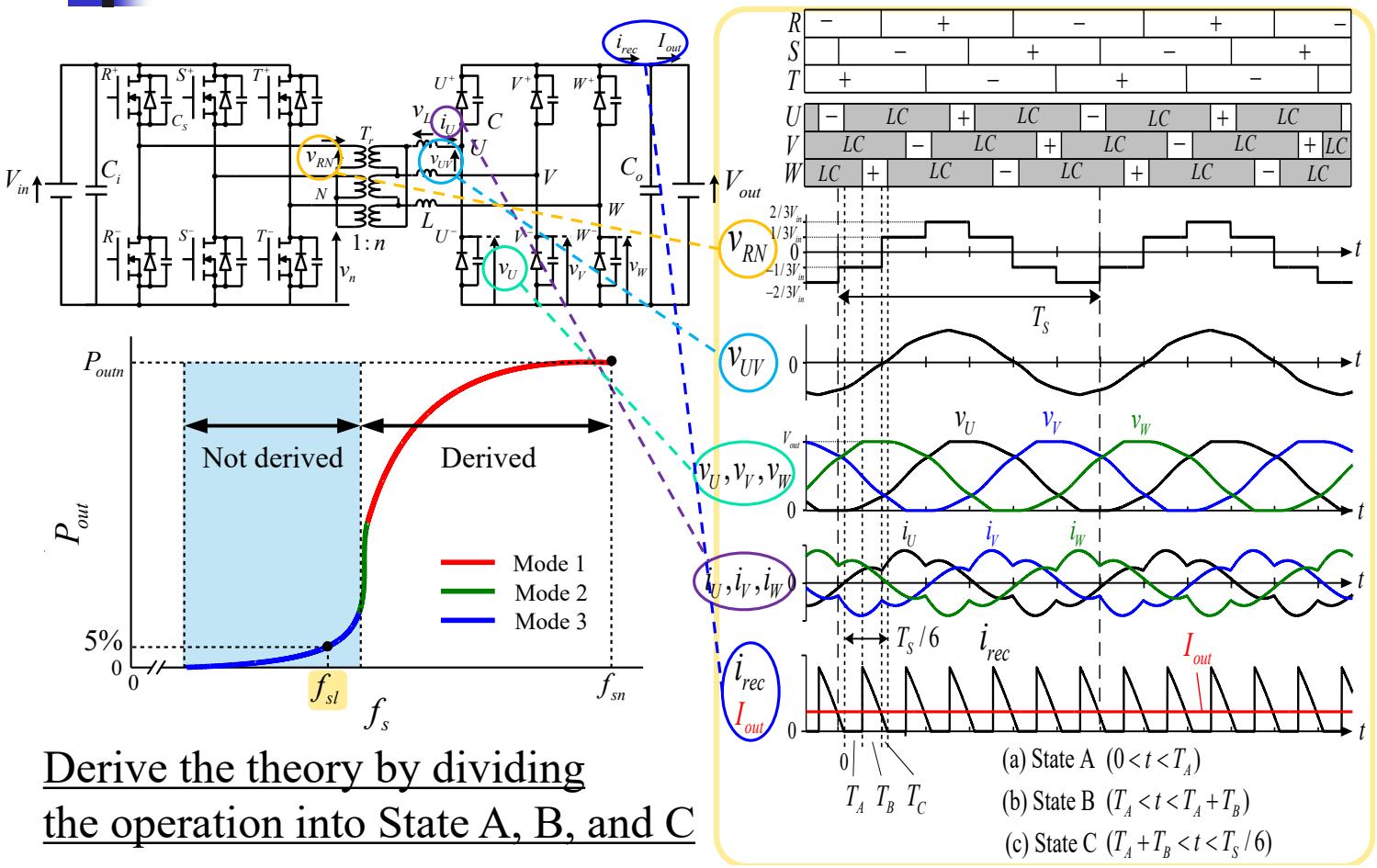
Resonant capacitor C is connected in parallel with the secondary-side diode
- LC resonance with leakage inductance L achieves high power factor
  → Transformer miniaturization
- Power transfer possible even when input voltage equals load voltage

⬇

Compact, high-efficiency, high-power circuit

△→◎

Theoretical waveforms (Mode 3)



Derive the theory by dividing the operation into State A, B, and C

Operating theory

＜Voltage equation of the transformer＞

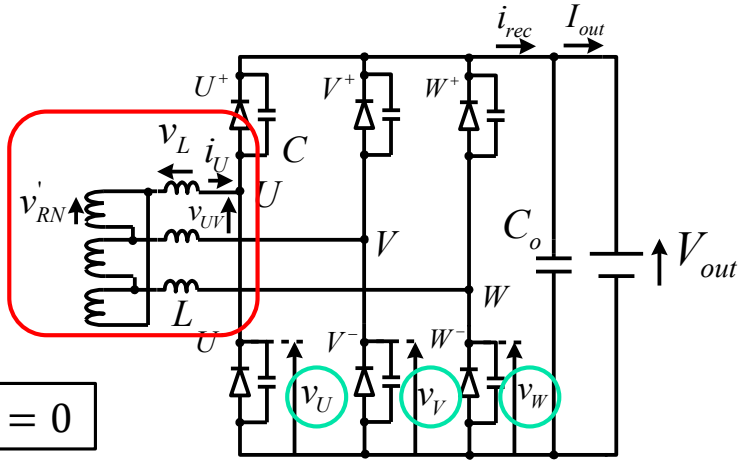
$$\begin{bmatrix} v'_{RN} \\ v'_{SN} \\ v'_{TN} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_U - i_V \\ i_V - i_W \\ i_W - i_U \end{bmatrix} + \begin{bmatrix} v_{UV} \\ v_{VW} \\ v_{WU} \end{bmatrix} \Rightarrow \begin{bmatrix} v'_{RN} - v'_{TN} \\ v'_{SN} - v'_{RN} \\ v'_{TN} - v'_{SN} \end{bmatrix} = 3L\frac{d}{dt}\begin{bmatrix} i_U \\ i_V \\ i_W \end{bmatrix} + \begin{bmatrix} v_{UV} - v_{WU} \\ v_{VW} - v_{UV} \\ v_{WU} - v_{VW} \end{bmatrix}$$

v'_{RN}: secondary–referred value of primary voltage v_{RN}

⇓

When the transformer turns ratio is n

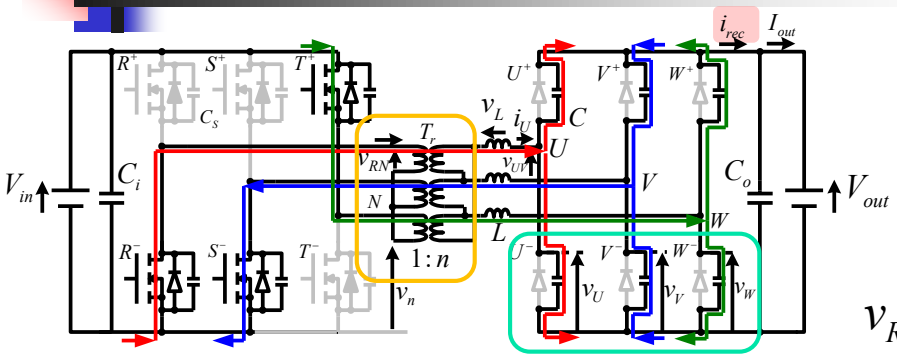
$v'_{RN} = n \times v_{RN}$

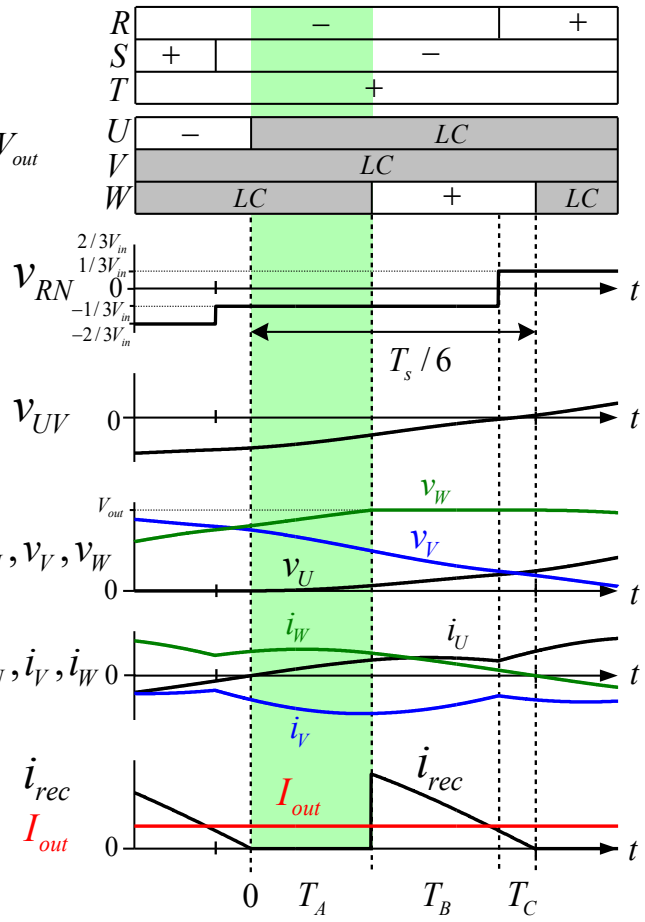


＜ Constraint condition ＞ $i_U + i_V + i_W = 0$

Theory derivation based on diode voltages v_U, v_V, and v_W

State A $(0 < t < T_A)$





★ No output current flow

$t = 0$: Start of U phase resonance

$\rightarrow t = T_A$: End of W phase resonance

$$v'_{RN} - v'_{TN} = n(-V_{in}/3 - 2V_{in}/3) = -nV_{in}$$

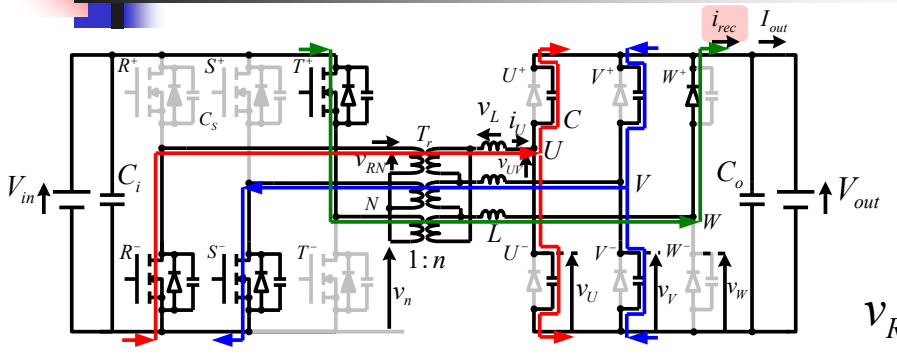
$$v_U(t) = \frac{1}{C}\int_0^{T_A} \frac{i_U(t)}{2}\,dt$$

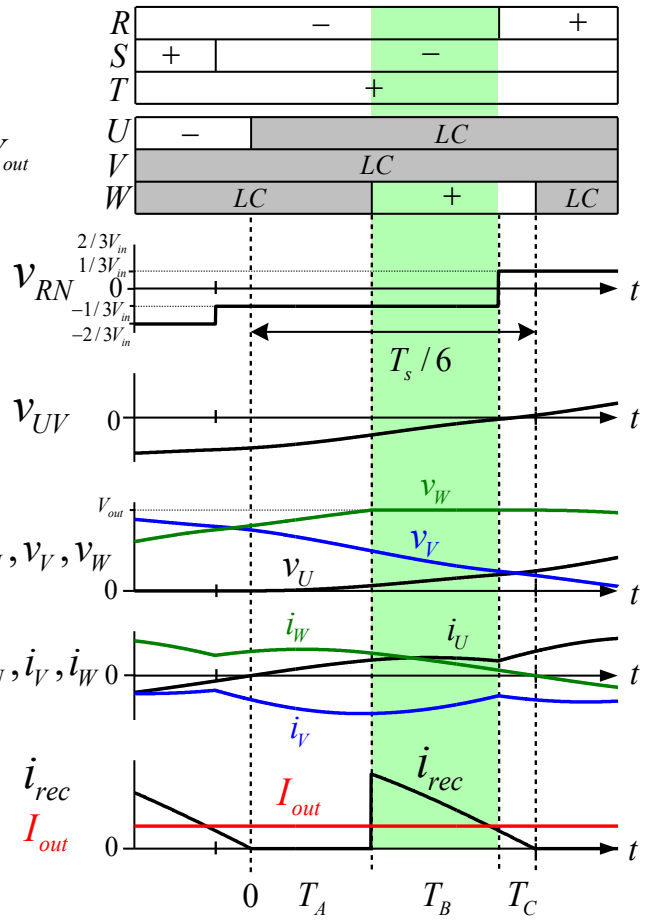
Initial value

$$v_V(t) = \frac{1}{C}\int_0^{T_A} \frac{i_V(t)}{2}\,dt + v_V(0)$$

$$i_{rec}(t) = 0$$

State B $(T_A < t < T_A + T_B)$





★ LC Resonance occurs in phases U, V

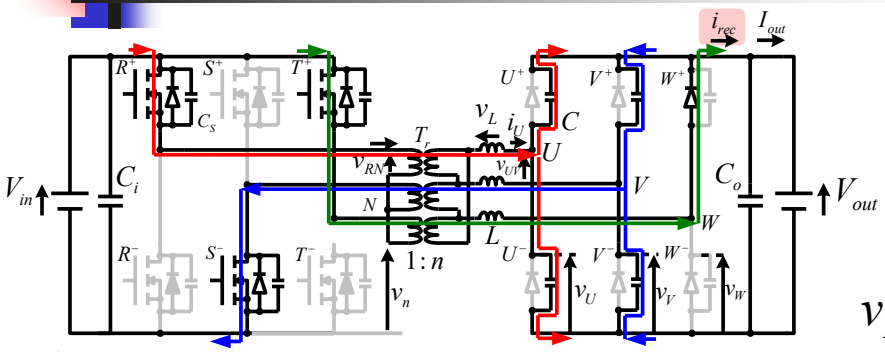
$t = T_A$: End of W phase resonance

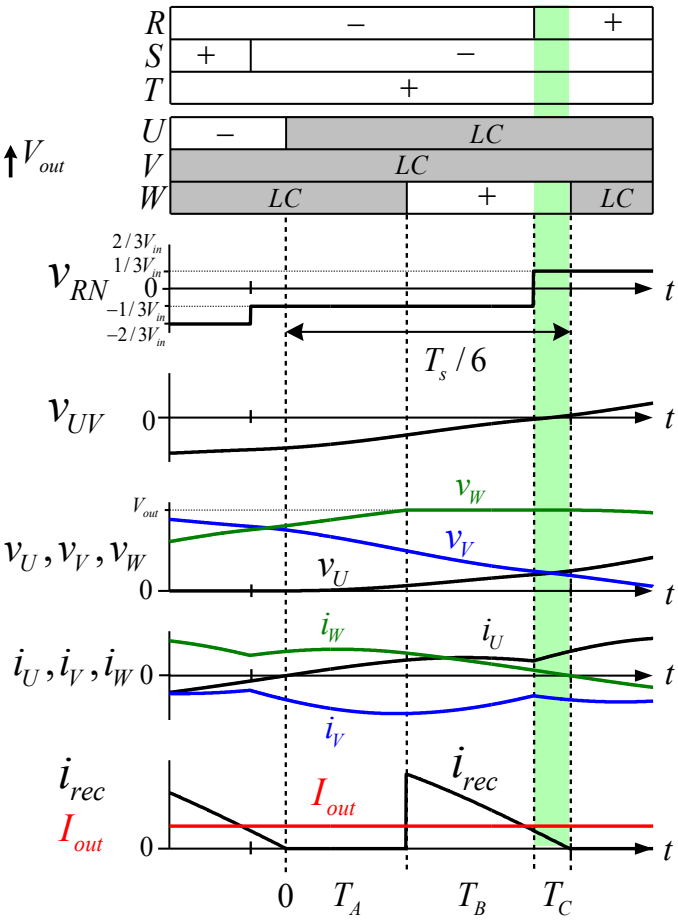
$\rightarrow t = T_A + T_B$: Switching of switch R

$$i_W(t) = \{3nV_{in} - 2V_{out} + v_U(T_A) + v_V(T_A)\}\sqrt{\frac{2C}{3L}}\sin\frac{t - T_A}{\sqrt{6LC}} + i_W(T_A)\cos\frac{t - T_A}{\sqrt{6LC}}$$

$$i_{rec}(t) = \frac{1}{2}i_U(t) + \frac{1}{2}i_V(t) + i_W(t) = \frac{1}{2}i_W(t)$$

State C ($T_A + T_B < t < T_s/6$)





★ Different switching state from State B, but same secondary-side resonance condition

$t = T_A + T_B$: Switching of switch R

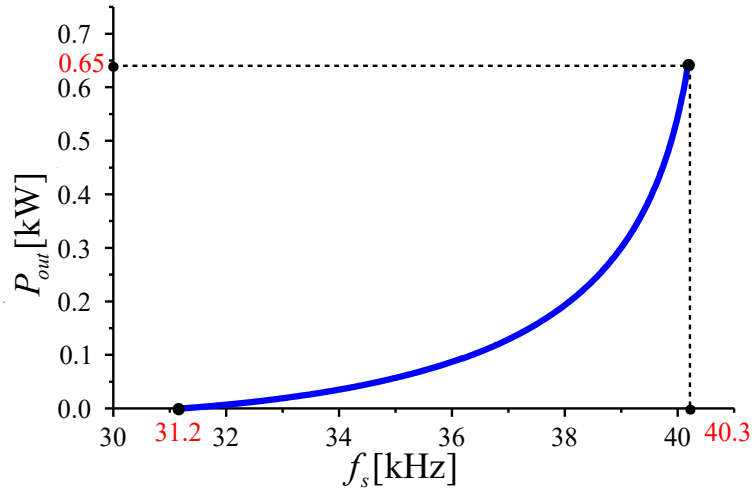
$\rightarrow t = T_s/6$: Start of phase-W resonance

$$i_W(t) = \{3nV_{in} - 2V_{out} + v_U(T_A + T_B) + v_V(T_A + T_B)\}\sqrt{\frac{2C}{3L}}\sin\frac{t - T_A - T_B}{\sqrt{6LC}} + i_W(T_A + T_B)\cos\frac{t - T_A - T_B}{\sqrt{6LC}}$$

$$i_{rec}(t) = \frac{1}{2}i_W(t)$$

Output power characteristics（Mode 3）

Parameters	Symbols	Values
Output Power	P_{out}	0 – 0.65 kW
Input voltage	V_{in}	250 V
Output voltage	V_{out}	250 V
Turn ratio of transformer	n	10/9
Leakage inductor	L	17 μH
Resonant capacitor	C	110 nF
DC capacitor	C_i, C_o	1500 μH



$$P_{out} = V_{out} \times I_{out} = V_{out} \times \frac{6}{T_s}\int_0^{T_s/6} i_{rec}(t)dt = 6V_{out}f_s\int_0^{T_s/6} i_{rec}(t)dt$$

- Output power can be controlled by transformer frequency f_s

⬇

Simple control using a single variable

- Wide-range power control through design of n, L, and C

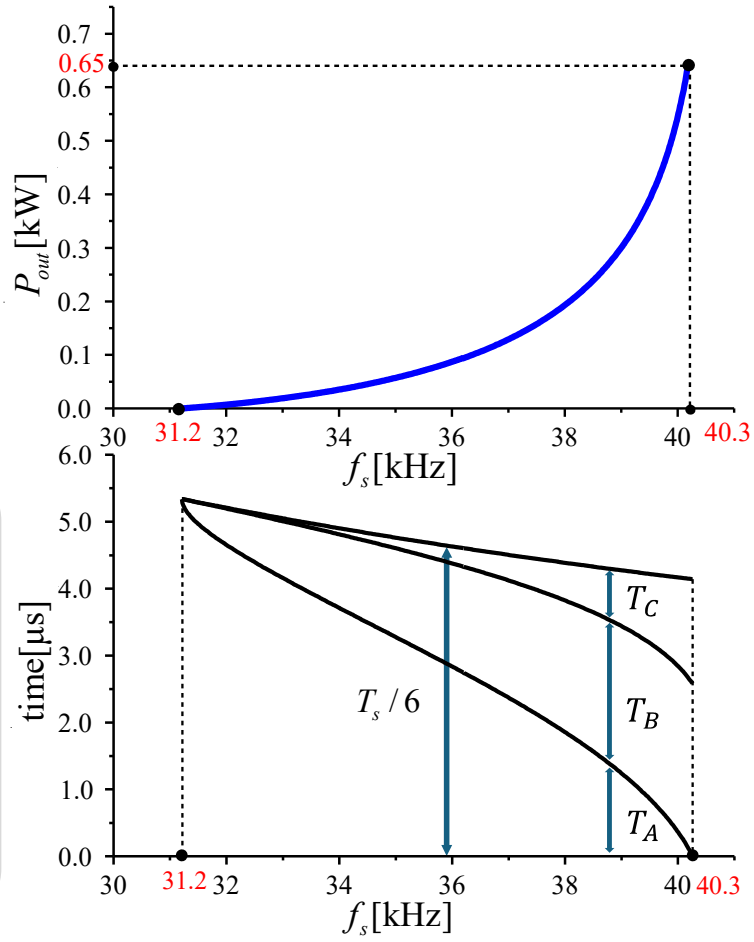
Output power characteristics（Mode 3）

Parameters	Symbols	Values
Output Power	P_{out}	0 – 3.7 kW
Input voltage	V_{in}	250 V
Output voltage	V_{out}	250 V
Turn ratio of transformer	n	10/9
Leakage inductor	L	17 μH
Resonant capacitor	C	110 nF
DC capacitor	C_i, C_o	1500 μH

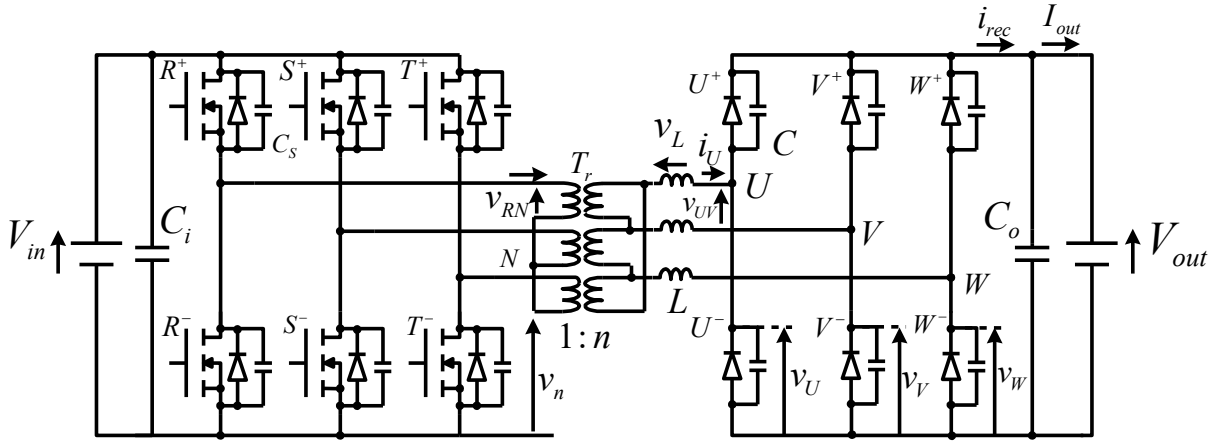
Lower frequency
→ Longer State A duration T_A relative to period T_s

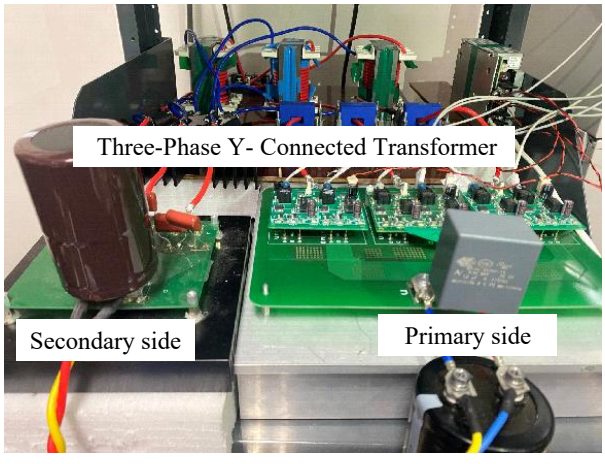
⬇

Reduced output-current conduction time
→ Lower output power



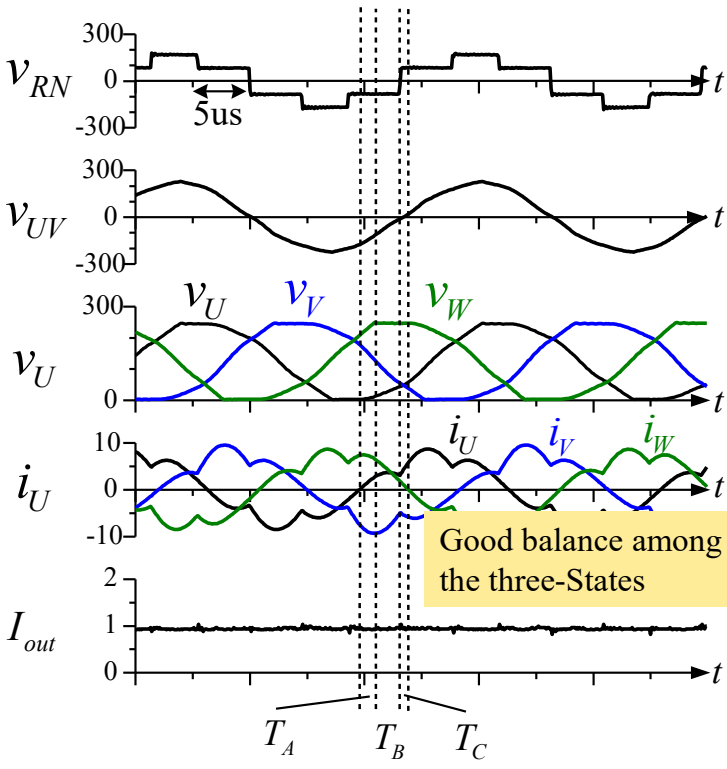
Experimental conditions



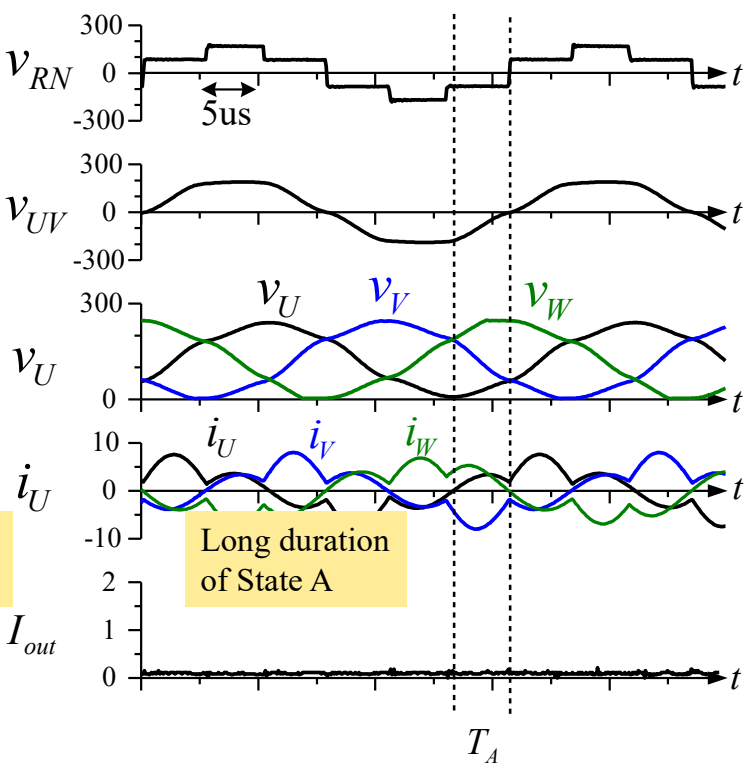


Parameters	Symbols	Values
Output Power	P_{out}	0 – 3.7 kW
Switching frequency	f_s	32 – 53 kHz
Input voltage	V_{in}	250 V
Output voltage	V_{out}	250 V
Turn ratio of transformer	n	10/9
Leakage inductor	L	17 μH
Resonant capacitor	C	110 nF
DC capacitor	C_i, C_o	1500 μH

Experimental waveforms

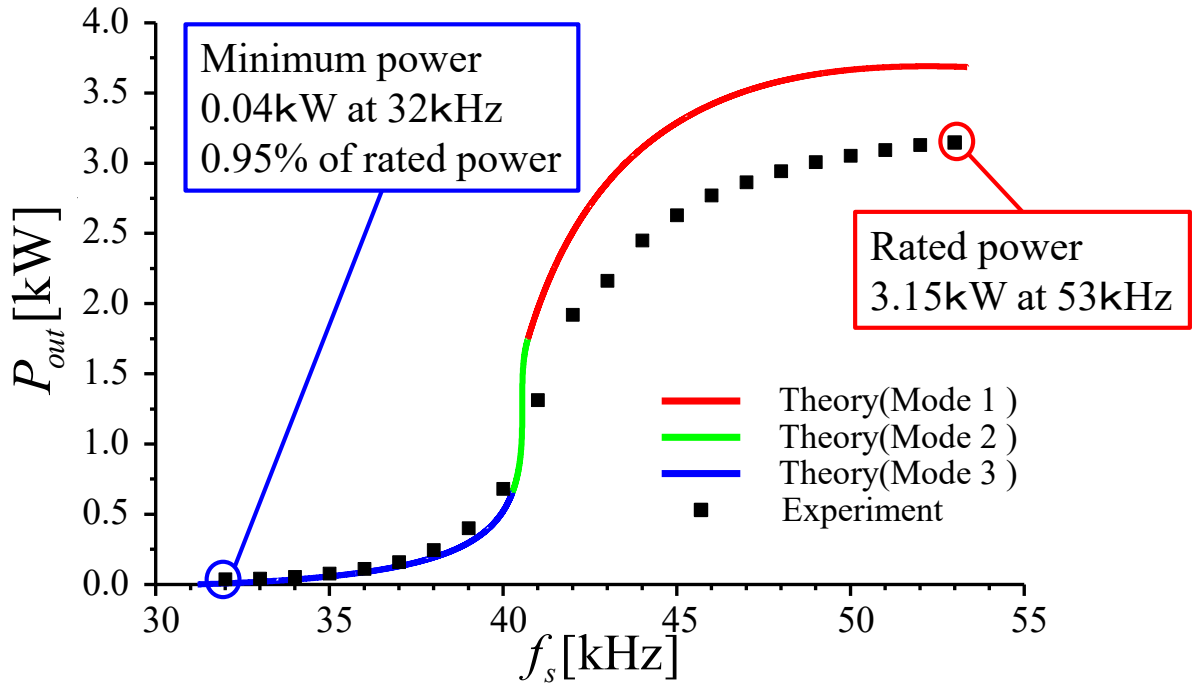


Fundamental waveform f_s =38 kHz
P_{out} = 0.247 kW, i_{out} = 0.99 A



Zero-power waveform f_s =32 kHz
P_{out} = 0.04 kW, i_{out} = 0.15 A

Experimental Results



- Theoretical and experimental results agree in Modes 2 and 3
- ▲ Large discrepancy in Mode 1

➡ Near rated power, large current causes voltage drops due to transformer winding resistance

Conclusions

Purpose

- Proposed SR-SAB converter achieves lower primary-side voltage rating, smaller transformer size, and higher efficiency than the conventional converter
- Theoretical derivation of low-power operation for circuit design enabling wide-range power control

Method

- Circuit operation analysis using transformer voltage equations

Result

- Low power characteristics of the proposed converter were theoretically derived
- Output power reduced to 0.95% of rated power in experiments

Coupled Inductor Design of Interleaved CF-DAB Converter for Fuel Cell

with Maxwell analysis

Gyeongsang National University
Power Electronics and Motion Control Lab.
Jeong-In Lee

Outline

1. Introduction
2. Interleaved CF-DAB converter with coupled inductor
3. Coupled inductor design of interleaved CF-DAB converter
4. Maxwell analysis result
5. Conclusion

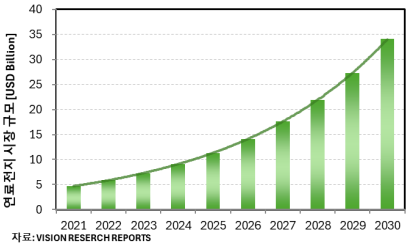
Introduction

❖ Fuel cell policy and market outlook

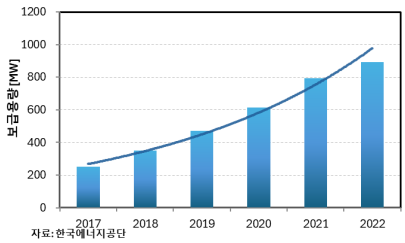
- Core technology for distributed/flexible power sources
- Continuous domestic policies related to hydrogen
- Global fuel cell market: $2.62 billion as of 2020
- Korean fuel cell market: Cumulative installed capacity of 611,568 kW as of 2020
- Diversification of application fields such as ships and drones

< Advantages of fuel cells>

< History of korea's hydrogen policy >



< Global fuel cell market outlook>

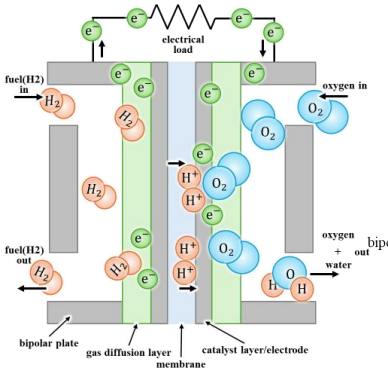


< Cumulative installed capacity of fuel cells(Korea)>

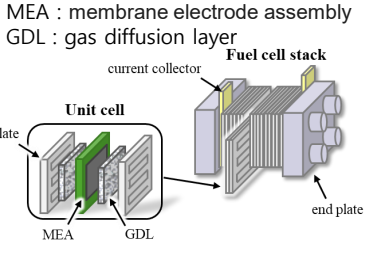
Introduction

❖ Fuel cell operating principles and electrical characteristics

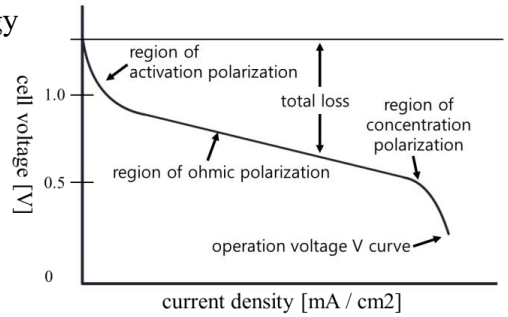
- Converts chemical energy: Hydrogen&Oxygen →Electrical energy
- Stack output volatage drops with increased load
- Low voltage/High current
- Load current ripple → Adversely affects fuel cell stack lifespan



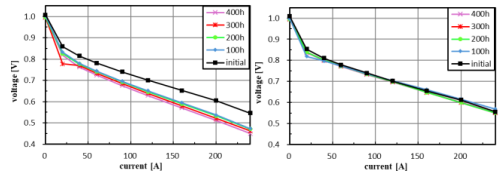
< Fuel cell operating principle>



< Structure of a fuel cell stack>



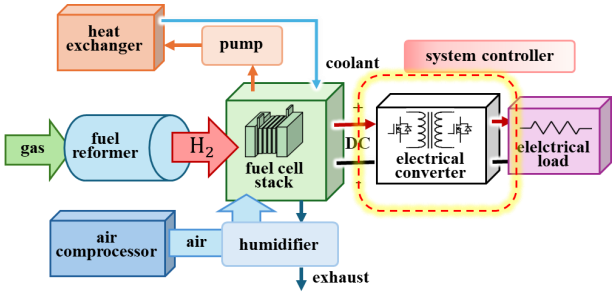
< I-V characteristic curve of fuel cell>



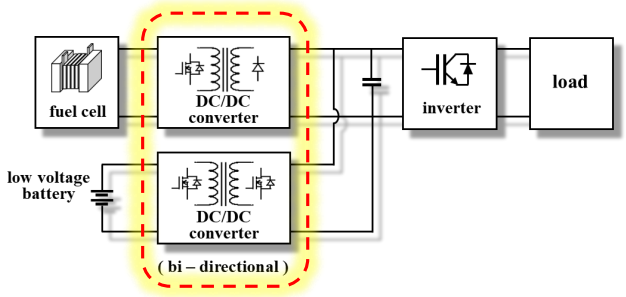
< Fuel Cell I-V Characteristic Curve >
(Left) Load variation, (Right) Constant current output

Introduction

- ❖ Components of the fuel cell system
  - Fuel cell stack, MBOP(Mechanical Balance of Plant), EBOP(Electrical Balance of Plant), control unit
  - EBOP: Converts the electrical energy output of the fuel cell stack into form suitable for load requirements
- ❖ Evaluation criteria for DC-DC converter for fuel cell system
  - High step-up and high efficiency
  - Low input current ripple
  - Wide input/output range



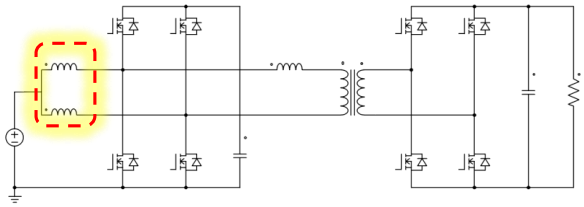
< Configurations of a Fuel cell system >



< Fuel cell and battery hybrid system EBOP configuration >

Introduction

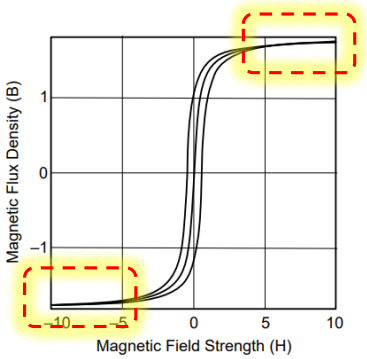
- ❖ 2-phase interleaved CF-DAB(Current Fed Dual Active Bridge)
  - Step-up topology; achieved high step-up
  - Soft switching(ZVS) operation; achieved high efficiency
  - Interleaving structure ; achieved low input current ripple
  - Fuel cell application systems; low voltage/high current



< 연료전지용 인터리브드 전류형 DAB 컨버터>

- ❖ Design precautions for 2-phase interleaved CF-DAB
  - Twice the number of components as single-phase
    - → Increased system volume
  - Low voltage/high current
    - → **High risk of input inductor saturation**

When fabricating a 2-phase interleaved CF-DAB, pay close attention to system size and input inductor saturation



< 코어 B-H 곡선>

Introduction

- Research on existing coupled inductor-based DC-DC converters
  - Interleaved CF-DAB based on coupled iductor
    - ➔ Integrate the CF-DAB input inductor into a coupled inductor
    - ➔ Reduce the number of magnetic elements → Reduce system volume
  - Interleaved CF-DAB based on dual coupled inductor
    - ➔ Integrate two input inductors, a transformer, and leakage inductance into two EE cores
    - ➔ Reduce system volume due to reduced losses and fewer magnetic elements

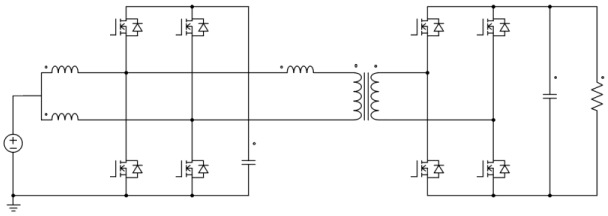
- **No suitability evaluation as a coupling inductor of DC-DC converter for fuel cells**

Introduction

- Mathematical modeling and design of coupled input inductor of interleaved CF-DAB
- Validation of the coupled input inductor design via Finite Element Analysis(FEA)
- Simulation analysis and validation of the interleaved CF-DAB converter with designed coupled inductor

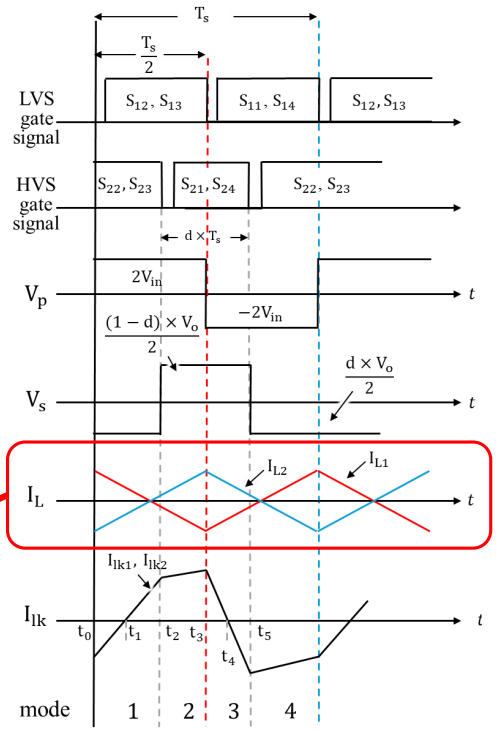
Interleaved CF-DAB converter with coupled inductor

- Interleaved CF-DAB
  - Interleaving operation with a 180-degree phase difference
  - Output control; the phase difference between the two bridges
  - Inductor current ripple in each phase cancels out
    → Low input current ripple
  - Step-up converter capable of ZVS
    → High efficiency/High step-up
- Output equations
  - $P_o = \frac{V_{in}V_o}{nfL_{lk}} \times \frac{\theta\cdot(\pi-\theta)}{\pi^2}$
  - $I_o = \frac{V_{in}}{nfL_{lk}} \times \frac{\theta\cdot(\pi-\theta)}{\pi^2}$



<Interleaved CF-DAB>

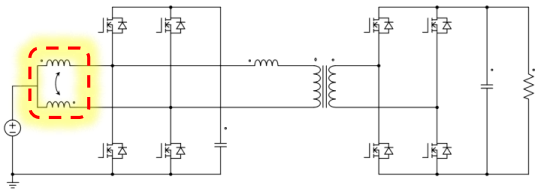
Current ripple cancellation



<Main waveforms>

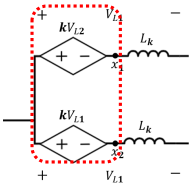
Interleaved CF-DAB converter with coupled inductor

- Interleaved CF-DAB wth coupled inductor
  - 2 input inductors
    → changed to 1 coupled inductor with a 1:1 turn ratio

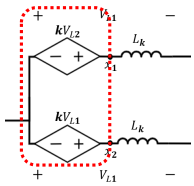


<Interleaved CF-DAB with coupled inductor>

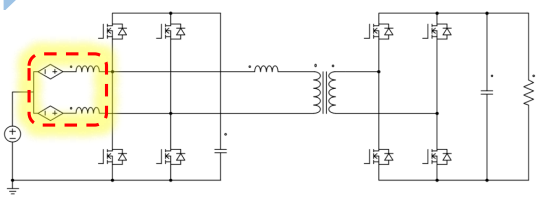
- Coupled inductor equivalent circuit
  - Representing the coupled inductor
    ➔ Dependent source and leakage inductance
  - The direction of th dependent source varies
    - Case 1: Directly coupled



    - Case 2: Indirectlty coupled



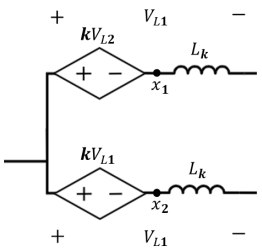
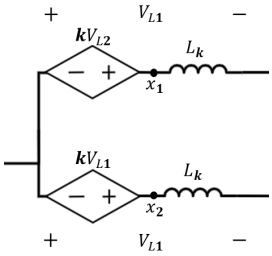
Equivalent circuit



<Coupled inductor equivalent circuit>

Interleaved CF-DAB converter with coupled inductor

❖ Comparison of characteristics based on coupling direction

	Directly coupled	Indirectly coupled
Equivalent circuit		
Features	- Alternating current component of the magnetic flux is canceld out - High effieiency by the core loss reduction - Core saturation risk increase	- DC component of the magnetic flux is canceled out - Core weight reduction by the core saturation risk decrease - High current ripple increase
Total magnetic flux Φ_m	$\Phi_m = \Phi_{21} + \Phi_{12}$	$\Phi_m = \Phi_{21} - \Phi_{12}$
Current ripple slope S of each phase inductor	$S = \frac{V_{in} - kV_{L2} - V_{L1}}{L_{lk}}$	$S = \frac{V_{in} + kV_{L2} - V_{L1}}{L_{lk}}$

Interleaved CF-DAB converter with coupled inductor

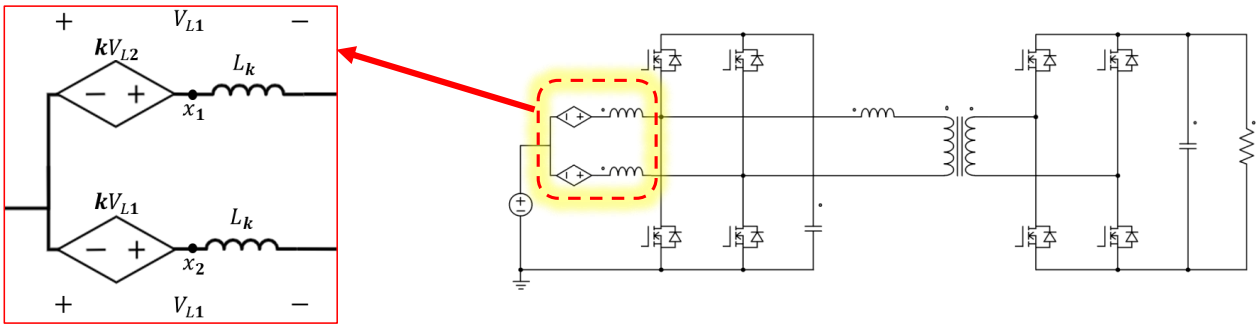
❖ Interleaved CF-DAB with indirect coupled inductor

□ Current ripple ΔI_L, ΔI_{in}

- $\Delta I_L = \frac{(1-k\cdot d_{LV}/(1-d_{LV}))V_{in}}{L_{lk}} \times d_{LV}T_s$
- $\Delta I_{in} = \frac{2(1+k)d_{LV}V_{in}}{(1-d_{LV})L_{lk}} \times (0.5 - d_{LV})T_s$

LV-side duty $d_{LV} = 0.5$

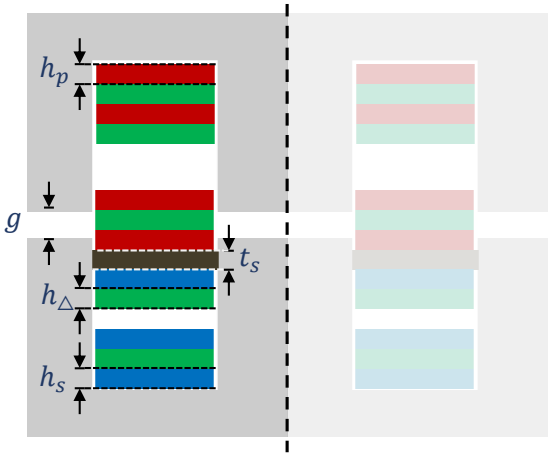
- $\Delta I_L = \frac{(1-k)V_{in}}{L_{lk}} \times \frac{T_s}{2}$
- $\Delta I_{in} = 0$



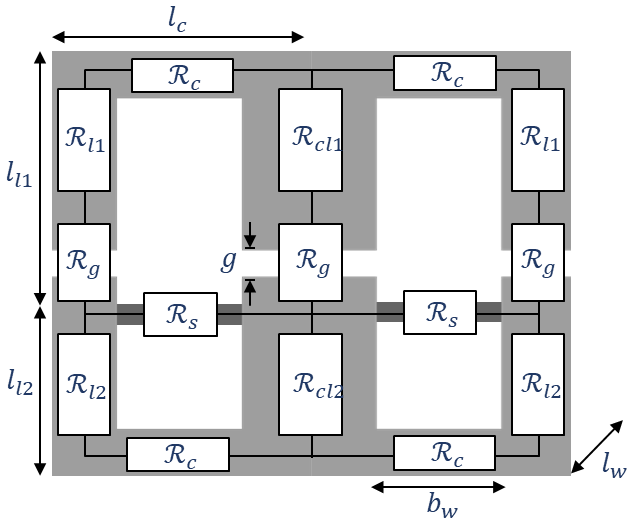
Coupled inductor design of interleaved CF-DAB converter

❖ Planar coupled inductor

- Configuration : Type E ferrite core, primary and secondary PCB windings, magnetic sheet
- Insertion of magnetic sheet between primary and secondary windings→ High leakage inductance
- Sufficient inter-winding spacing → Copper losses due to proximity effects negligible
- **Small volume**
- **High reproducibility → Suitable for interleaved converter reauiring identical specifications**



<Planar coupled inductor structure>



<Planar coupled inductor magnetic circuit>

Coupled inductor design of interleaved CF-DAB converter

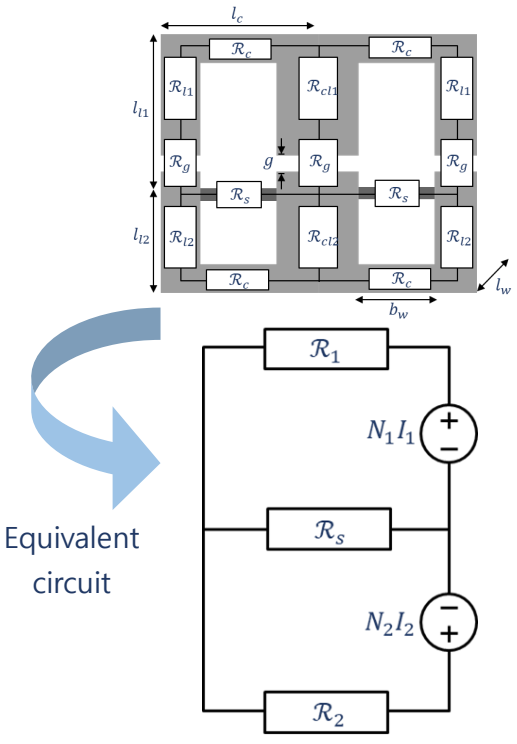
❖ Inductance of planar coupled inductor

- $L_m = \frac{N^2}{\mathcal{R}_1} \parallel \left(L_{lk} + \frac{N^2}{\mathcal{R}_2}\right) - \left(\frac{N^2}{\mathcal{R}_1} \parallel L_{lk}\right) \cong \frac{N^2}{\mathcal{R}_1} - \left(\frac{N^2}{\mathcal{R}_1} \parallel L_{lk}\right)$
- $L_{lk} = L_{ksh} + L_{kw} \cong L_{ksh}$
- $L_{ksh} = 2\mu_0\mu_r \times \frac{{F_s}^2 A_s}{I_1^2 b_w}$

❖ Reluctance calculation

- $\mathcal{R}_1 = \frac{2g}{\mu_0 A_g} + \frac{l_1}{\mu_0\mu_r A_c}$
- $\mathcal{R}_2 = \frac{l_2}{\mu_0\mu_r A_c}$
- $\mathcal{R}_s = \frac{b_w}{\mu_0\mu_s A_s} = \frac{b_w}{\mu_0\mu_r l_w t_s}$
- $l_1 = l_c + 2l_{l1}$
- $l_2 = l_c + 2l_{l2}$

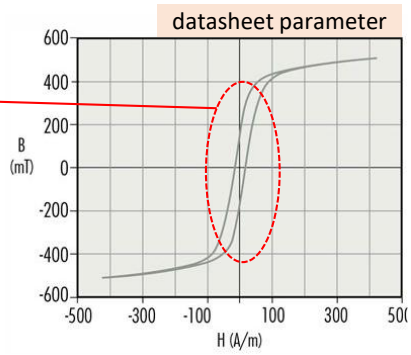
L_{ksh}: Leakage inductance due to magnetic sheet
L_{kw}: Leakage inductance from windings and insulator
N: Inductor turns



<Magnetic equivalent circuit>

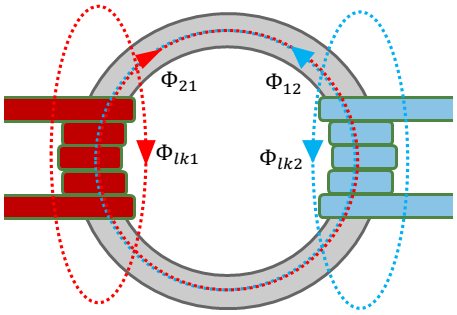
Coupled inductor design of interleaved CF-DAB converter

- Saturation of the magnetic core
  - $\Phi_{sat} = A_c \times B_{sat}$
  - $I_{sat} = \frac{NA_c}{L_m} \times B_{sat}$



< Core B-H curve>

- Magnetic design of a indirectly coupled inductor
  - $\Phi_m = \Phi_{21} - \Phi_{12}$
    → Where, since the MMF of the two winding ar the same
    → $\Phi_{21} = \Phi_{12}$
    → Thus, $\boldsymbol{\Phi_m = 0}$
  - Magnetic field strength H
    → $H_{max} = 2 \cdot \pi \cdot \frac{N \cdot \Delta i_L}{l_e}$
    → $H_{min} = -2 \cdot \pi \cdot \frac{N \cdot \Delta i_L}{l_e}$

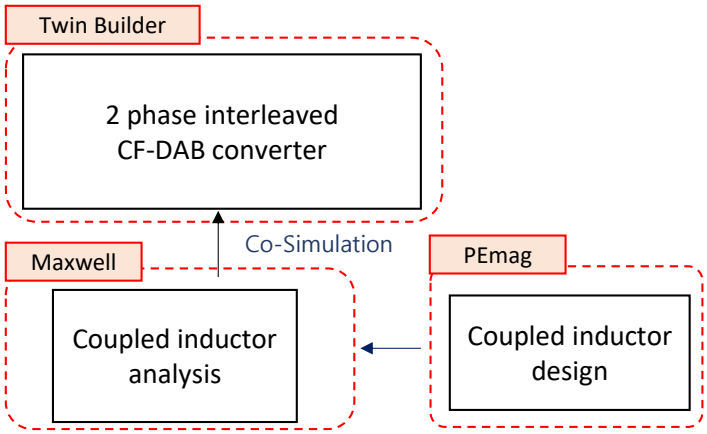


< Core flux flow diagram>

Φ_{sat}: Core saturation magnetic flux
I_{sat}: Core saturation current
B_{sat}: Core saturation magnetic flux density

Maxwell analysis result

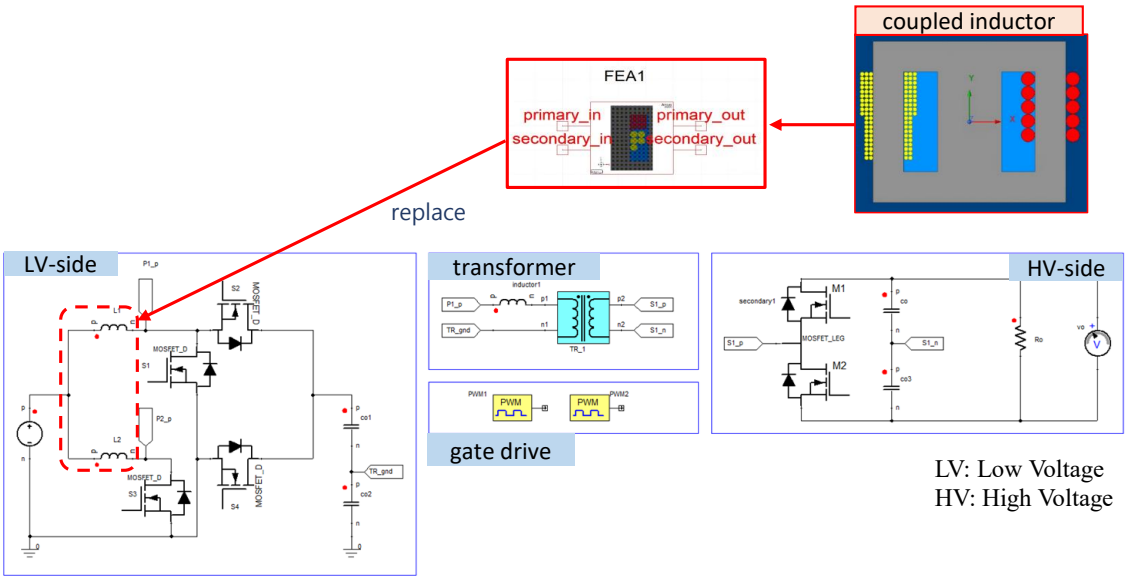
- Ansys/Maxwell
  - Finite Element Analysis(FEA)
  - Co-simulation analysis



- Evaluation indicators
  - Inductor flux density
  - Input current ripple and phase current ripple
  - Converter input/output voltage/current

Maxwell analysis result

- Simulation specifications
  - 2-Phase interleaved CF-DAB converter
  - 1kW, input voltage: 50V → output voltage: 300V
  - Modeling with Ansys/Maxwell
    → 2-Phase CF-DAB simulation via Co-Simulation



<Simulation curcuit>

Maxwell analysis result

- Inductor specifications

Item	Saparated inductors	Coupled inductor	
Core	0077439A7	CR45810EC	
Input inductance	108.2uH	108.6uH	k = 0.85
Turns	31 turn	10 turn	
Magnetic sheet	-	EFW-02-240X80-T0800	
I_{sat}	15 A	15 A	

Conclusion

- Presentation of mathematical modeling/design of the coupled inductor for the interleaved CF-DAB converter
- Verification of feasibility as the MBOP for fuel cells through Maxwell simulation analysis
- Future review of validity through prototype fabrication and experimentation

Thank you for your attentions

Any Questions?

Gyeongsang National University
Power Electronics & Motion Control Lab.

A Study of Conducted Noise Overlap and Modeling in Multiple Inverters Considering Positions

Yuta Kobayashi*, Wataru Kitagawa
Nagoya Institute of Technology, Japan

May 14, 2026

JUSW2026[1]

Contents

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Research Background

Research Background

With the spread of power semiconductors, there has been an increase in cases where multiple power converters operate in closeness

Issues

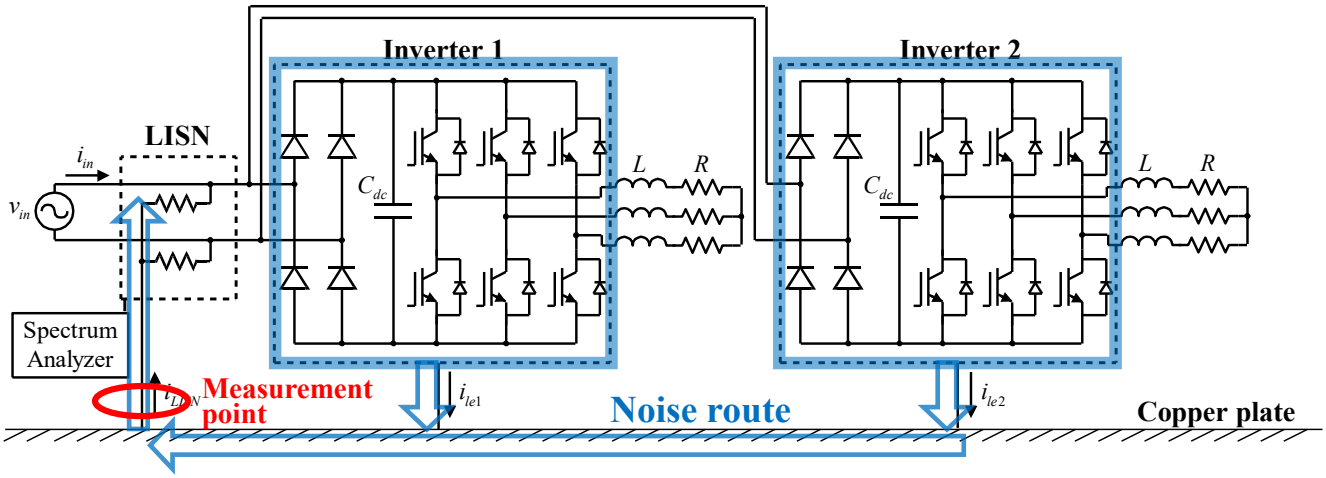
The superposition and interference of conducted noise during multi-unit drive, which vary depending on the positional relationship, necessitate the development of a new simulation methodology

Purpose

Proposal of a conducted noise superposition modeling method
Evaluating noise overlap from power converter positioning

Contents

Experimental Environment and Conditions



Input voltage v_{in}	100 V
Input current i_{in}	5.18 A
DC bus capacitor C_{dc}	1360 μF
Switching frequency f_s	12.5 kHz
AC frequency f	100 Hz
Load R , L	8 Ω , 2 mH
Output power P_{out}	326 W

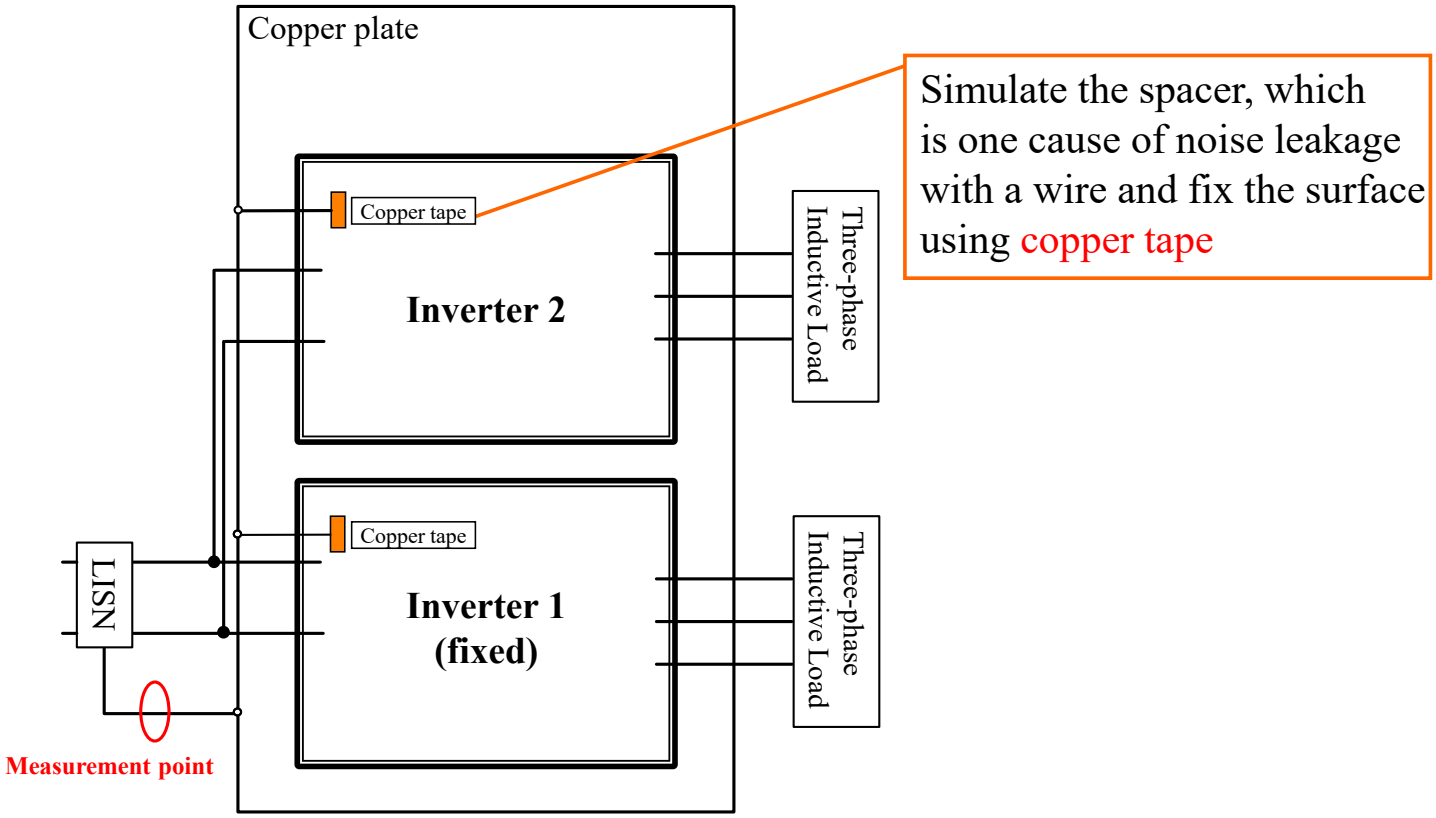
Measurement and analysis flow

- Connect Inverters surface and copper plate with a wire
- Measure leakage current into LISN
- Apply FFT analysis to leakage current

→Leakage current is analyzed at specific events to ensure consistent conditions

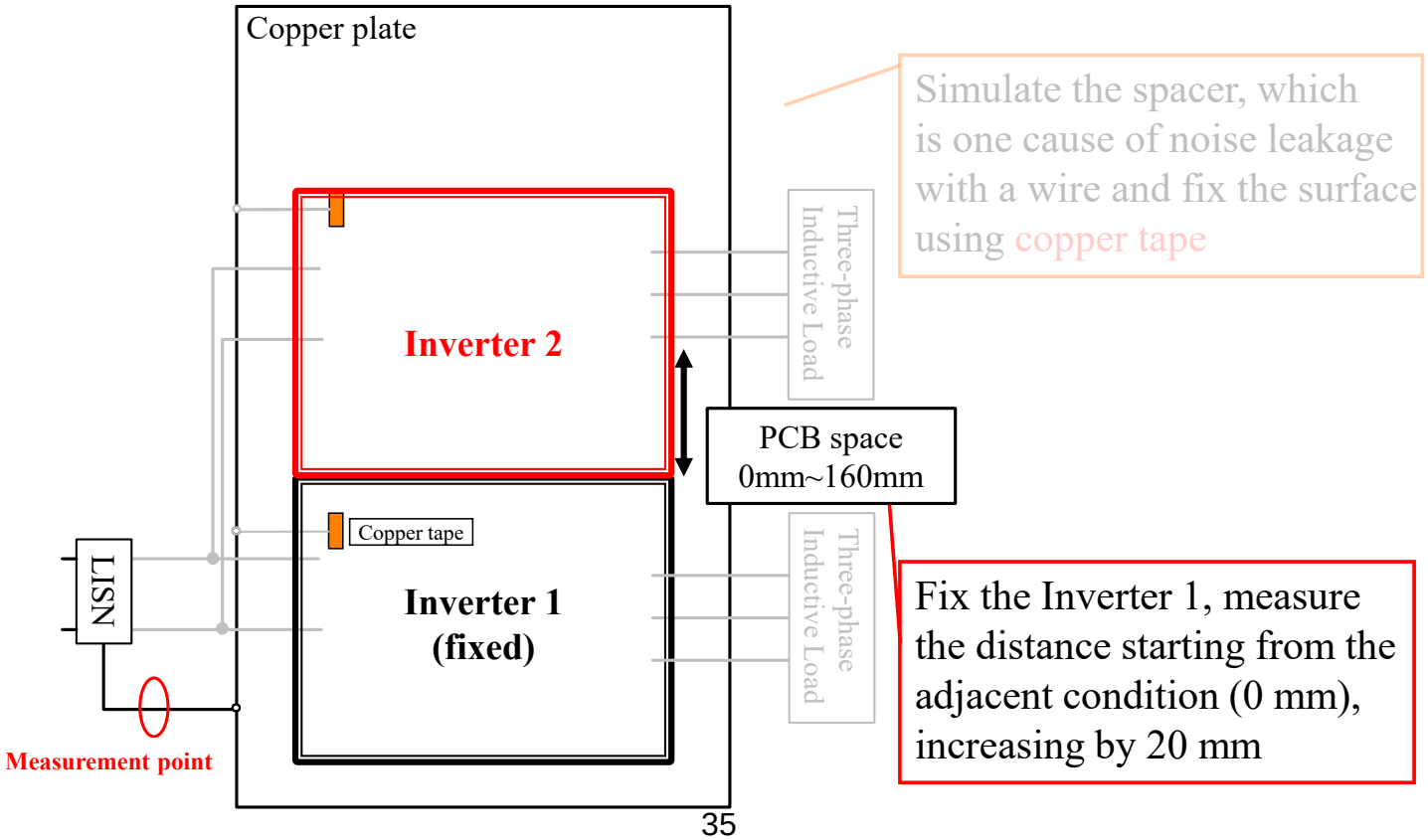
Experimental Environment and Conditions

Experimental Outline



Experimental Environment and Conditions

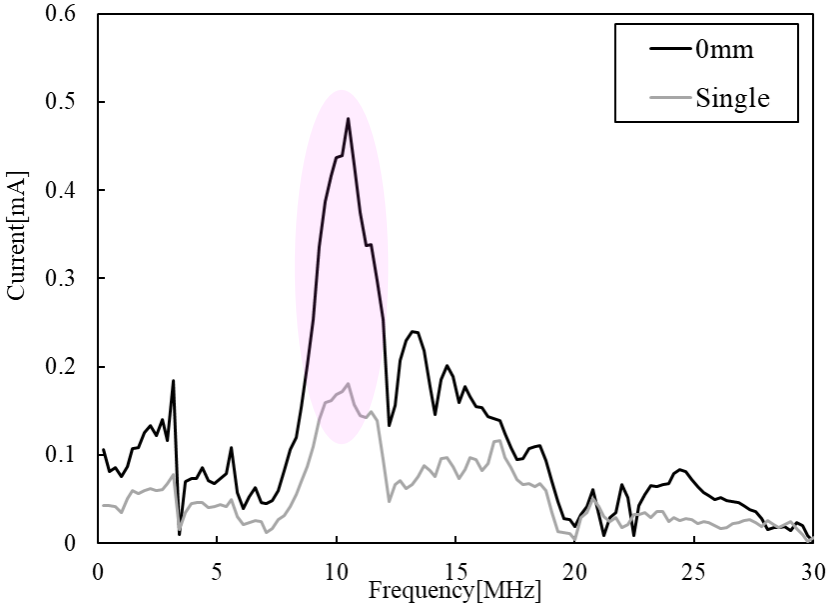
Experimental Outline



Contents

Comparison of Experimental Results

FFT analysis of leakage current



FFT amplitude of current

Condition	Max amplitude
0 mm	0.48 mA
Single Drive	0.18 mA

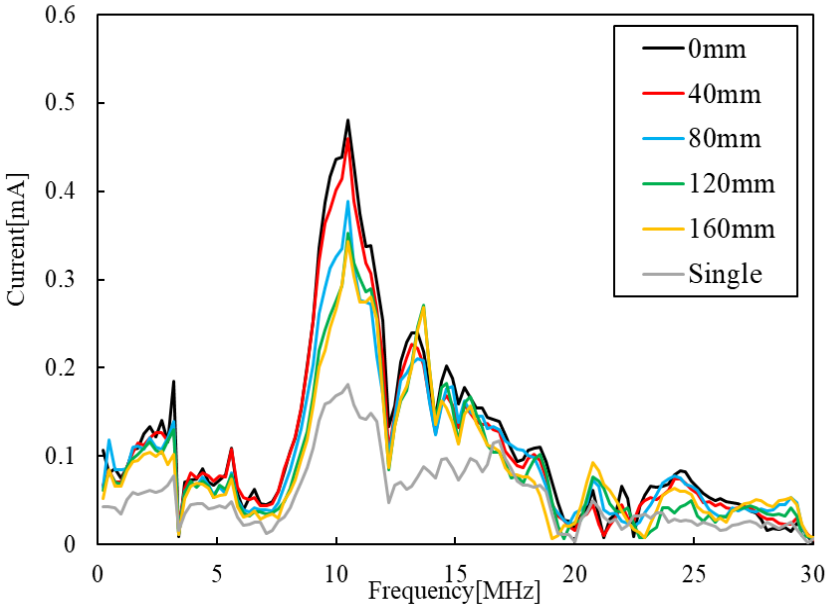
Current waveform amplitude

Condition	Max amplitude
0 mm	13.3 mA
Single Drive	6.36 mA

Noise superposition increases the overall current amplitude

Comparison of Experimental Results

FFT analysis of leakage current

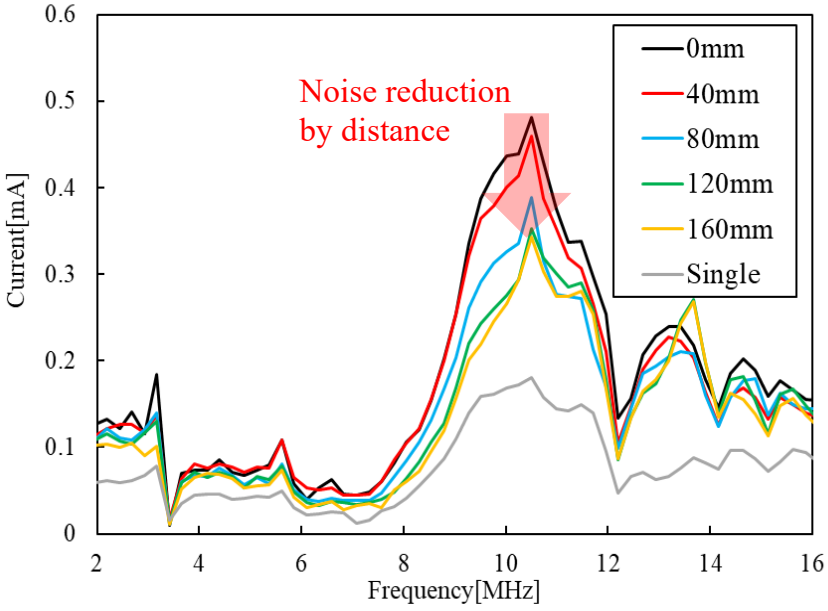


FFT amplitude of current

Condition	Max amplitude
0 mm	0.48 mA
40 mm	0.46 mA
80 mm	0.39 mA
120 mm	0.35 mA
160 mm	0.34 mA
Single Drive	0.18 mA

Comparison of Experimental Results

FFT analysis of leakage current(2 ~ 16 MHz)



FFT amplitude of current

Condition	Max amplitude
0 mm	0.48 mA
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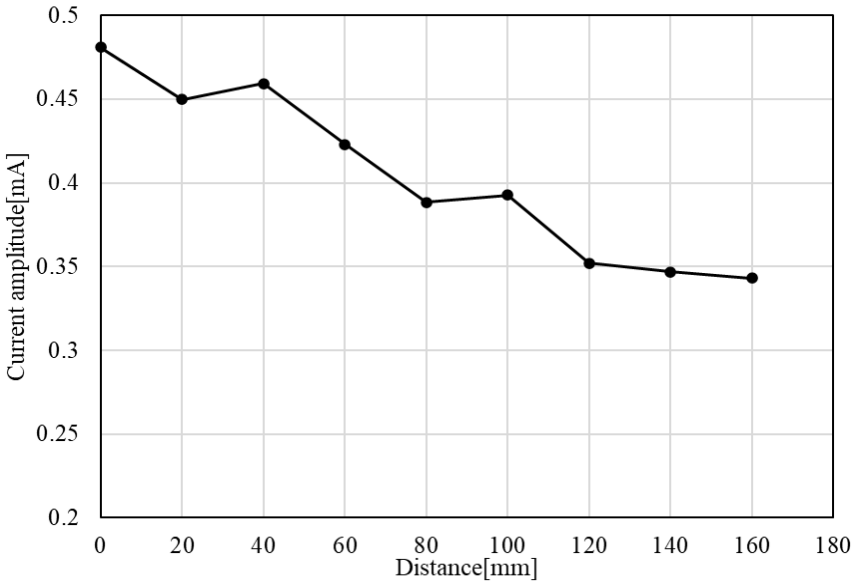
At the distance increase, the noise tends to decrease

Comparison of Experimental Results

■ Variation of current amplitude with distance



■ FFT amplitude of current

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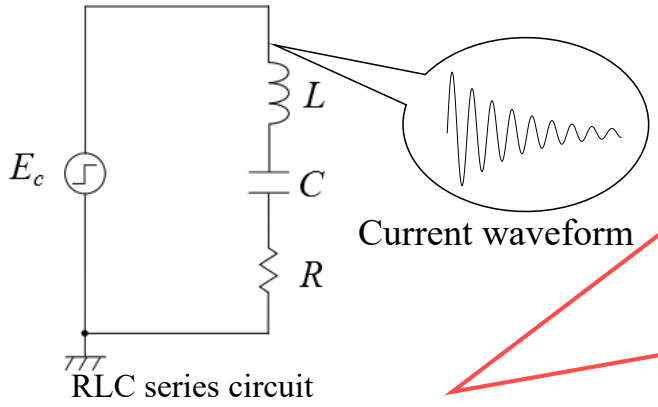
At the distance increase, the noise tends to decrease

Contents

Modeling Circuit

RLC series circuit

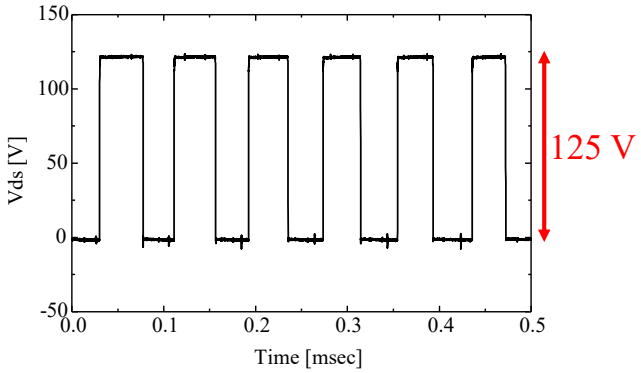


$$i(t) = \frac{E_c}{Z_0} e^{-\zeta \omega_n t} \sin \omega_n t$$

$$\omega_n = 2\pi f \quad , Z_0 = \frac{E_c}{i_{peak}} \quad , \zeta = \frac{R}{2Z_0}$$

ω_n : Natural Vibration Frequency
Z_0 : Characteristic Impedance
i_{peak} : Maximum Value of Current
ζ : Attenuation Coefficient

Determination of step voltage source E_C

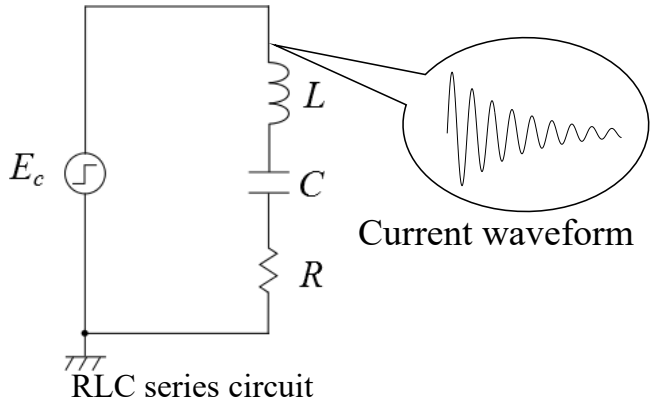


Measurement result of drain-source voltage

$$E_c = 125 \text{ V}$$

Modeling Circuit

RLC series circuit



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ω_n : Natural Vibration Frequency
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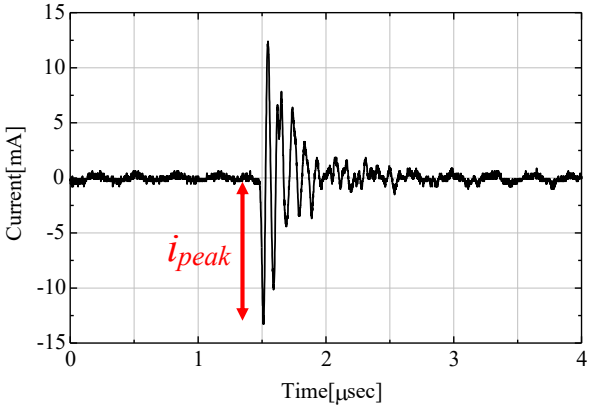
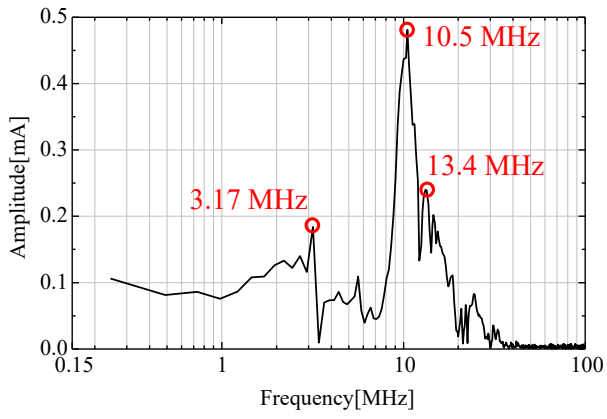
Analysis target (0 mm)



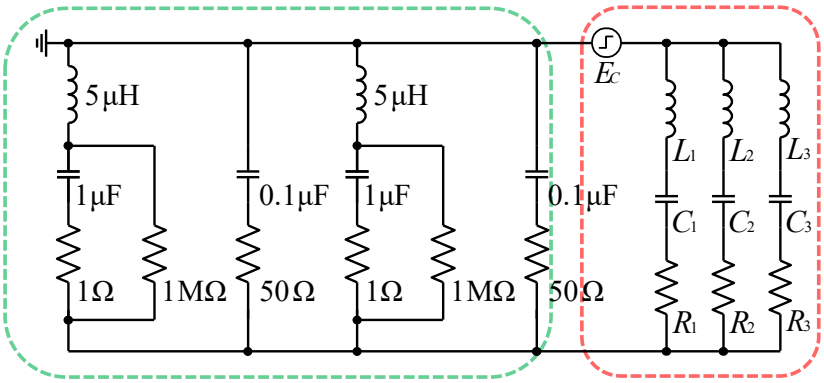
FFT analysis result (0 mm)



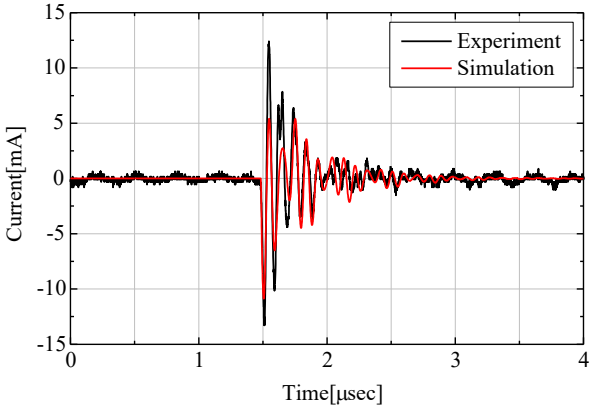
Simulation Result (PCB space 0 mm)

Simulation circuit

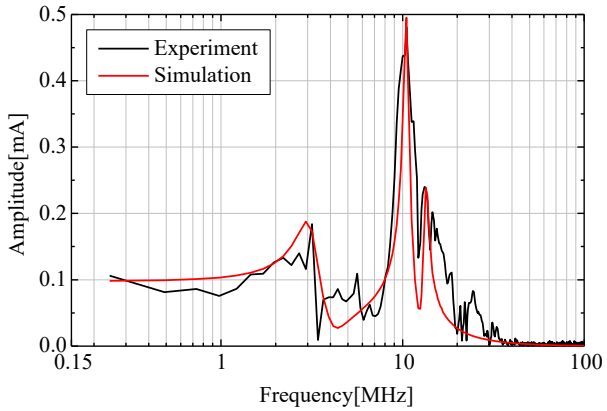
Equivalent circuit of LISN　　Modeling circuit



Leakage current simulation



FFT analysis simulation



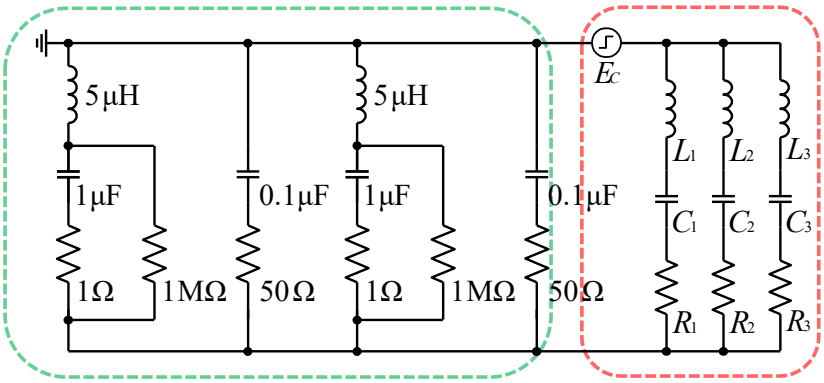
Circuit parameters (0 mm)

f	3.17 MHz	10.5 MHz	13.4 MHz
E_C	125 V	125 V	125 V
i_{peak}	2.71 mA	7.06 mA	3.51 mA
ω_n	19.9 Mrad/s	66.0 Mrad/s	84.4 Mrad/s
Z_0	46.1 kΩ	17.7 kΩ	35.6 kΩ
L_1, L_2, L_3	2.32 mH	0.268 mH	0.422 mH
C_1, C_2, C_3	1.09 pF	0.857 pF	0.333 pF
R_1, R_2, R_3	13.3 kΩ	1.31 kΩ	2.28 kΩ

Simulation Result (PCB space 160 mm)

Simulation circuit

Equivalent circuit of LISN　　Modeling circuit



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Simulation Result (PCB space 160 mm)

Simulation circuit

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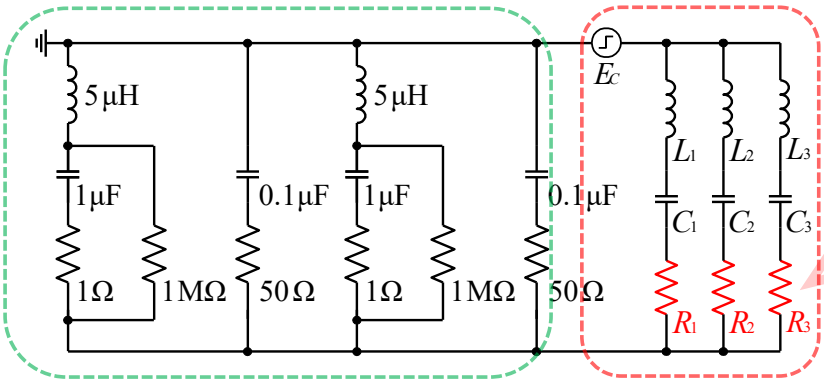

Simulation Approach

Simulations were performed by varying only the R, based on the 0 mm parameters and FFT results

Circuit parameters (160 mm)

f	3.17 MHz	10.5 MHz	13.4 MHz
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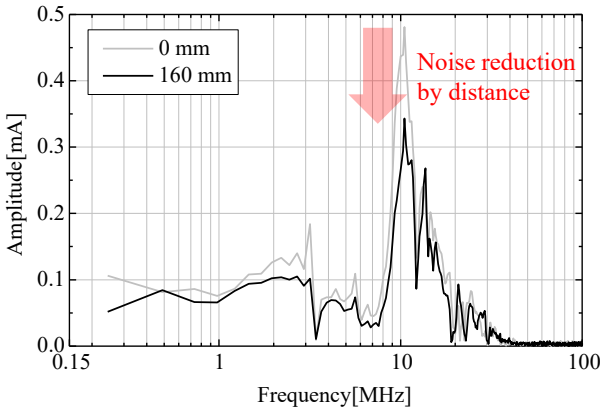
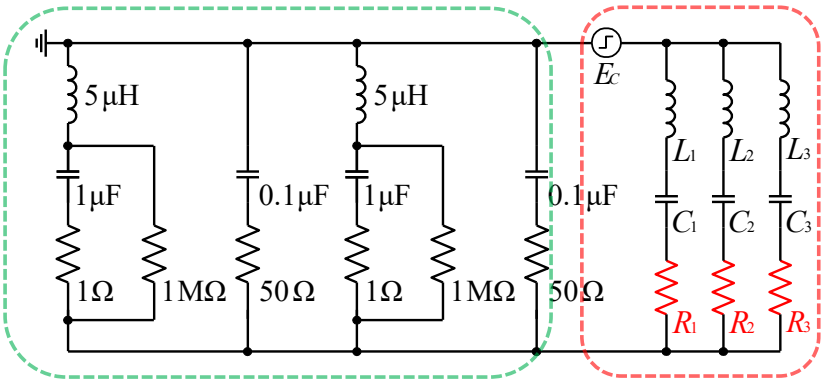
FFT analysis result



Simulation Result (PCB space 160 mm)

Simulation circuit

Equivalent circuit of LISN　　Modeling circuit



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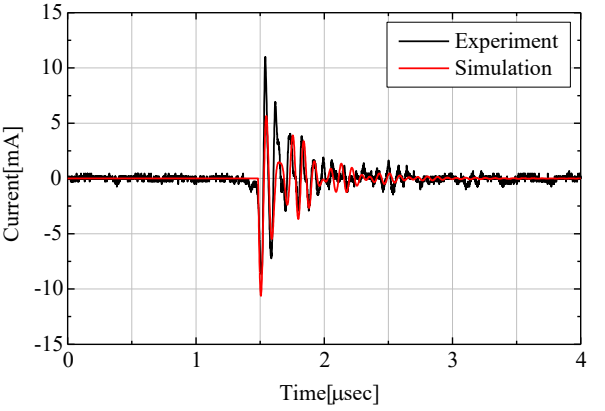
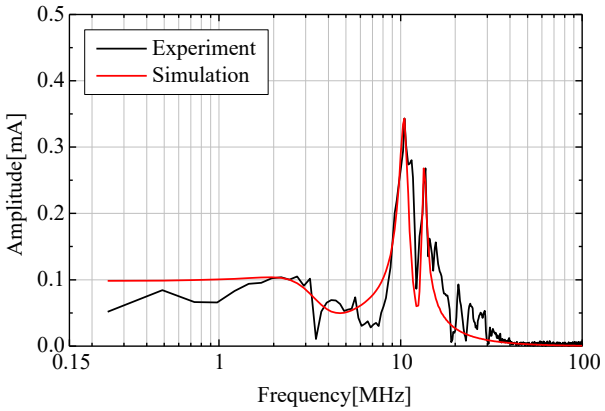
L_1, L_2, L_3	2.32 mH	0.268 mH	0.422 mH
C_1, C_2, C_3	1.09 pF	0.857 pF	0.333 pF
R_1, R_2, R_3	**40.0 kΩ**	**1.92 kΩ**	**2.03 kΩ**

Leakage current simulation

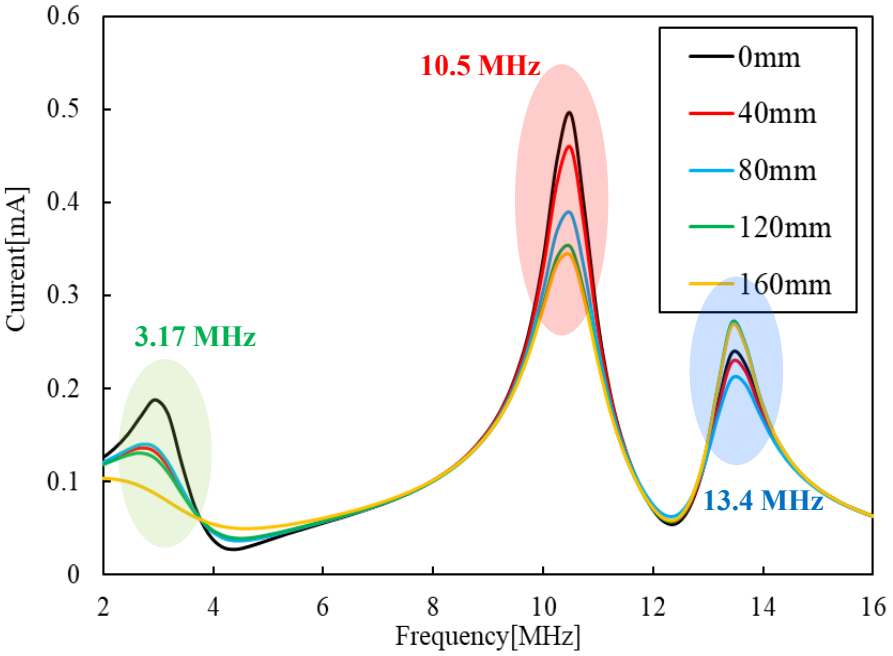


FFT analysis simulation



Simulation Results Comparison

■ FFT analysis of leakage current(2 ~ 16 MHz)



<u>Primary resonance</u> (10.5 MHz)

The amplitude gradually decreases as the distance increases

Minor resonance (13.4 MHz)

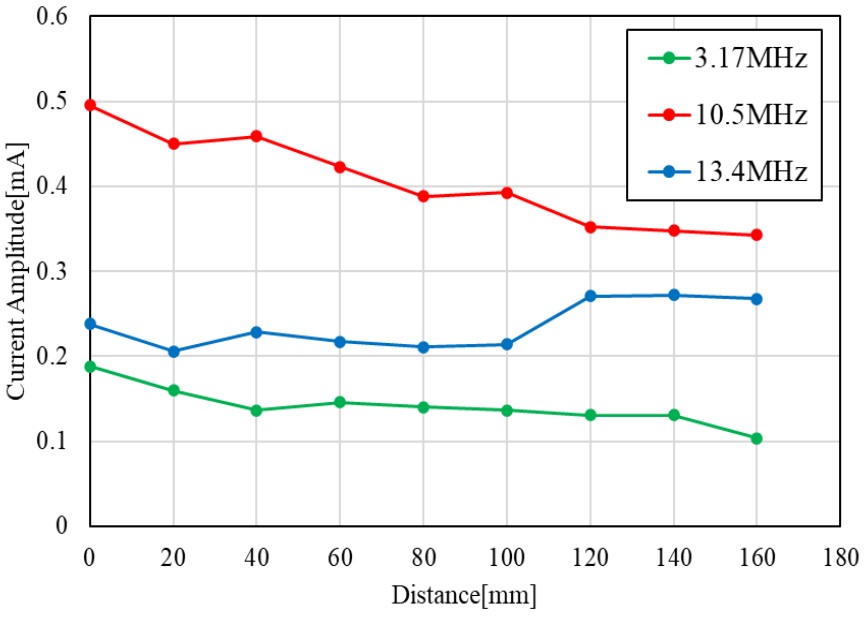
The amplitude remains relatively stable until 100mm, after which it surges rapidly

Minor resonance (3.17 MHz)

The amplitude gradually decreases as the distance increases

Simulation Results Comparison

■ Variation of current amplitude with distance



<u>Primary resonance</u> (10.5 MHz)

The amplitude gradually decreases as the distance increases

Minor resonance (13.4 MHz)

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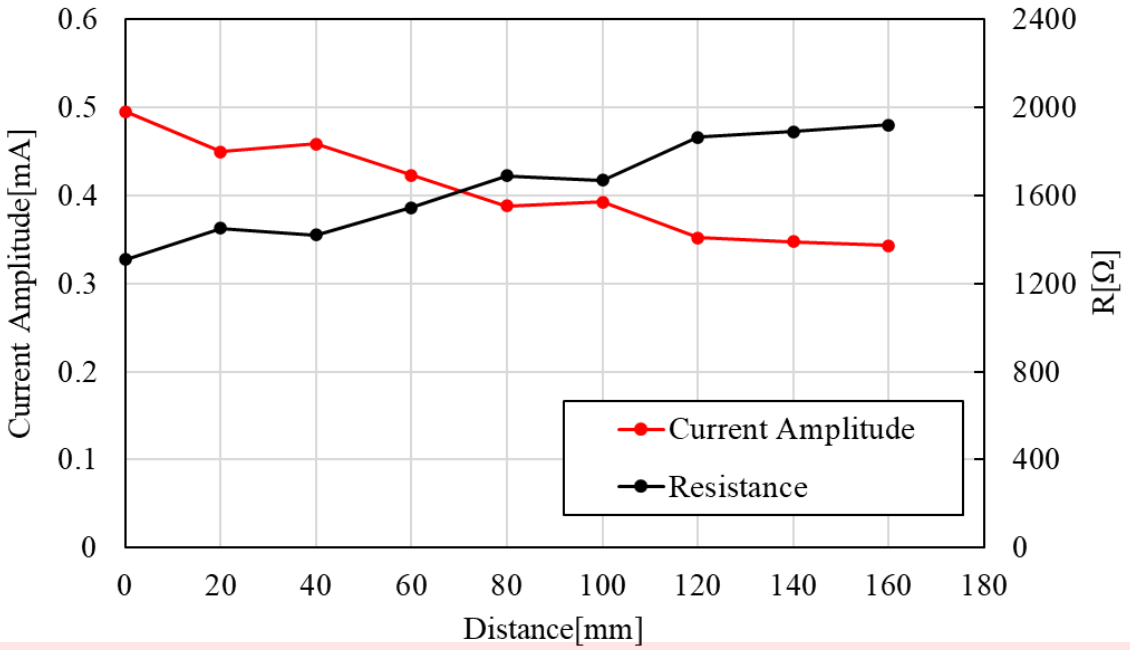
Minor resonance (3.17 MHz)

The amplitude gradually decreases as the distance increases

Correlation of Distance and R

■ **Relationship between resistance and current amplitude at Primary resonance**



At the distance increase, the resistance *R* increases linearly

Contents

Conclusion

Research

- Proposal of a conducted noise superposition modeling method
- Evaluating noise overlap from power converter positioning

Results

- Derived the high-frequency equivalent circuit from leakage current, and confirmed the usefulness of this method based on simulation results
- Confirmed noise variation depending on positional conditions
- Confirmed correlation between resistance and distance

Future Work

- Improving the accuracy of equivalent circuit
- Filter-insertion experiments and analysis
- Applying Genetic Algorithm to the modeling circuit

Analysis of Gate Drive Circuit for GaN HEMT

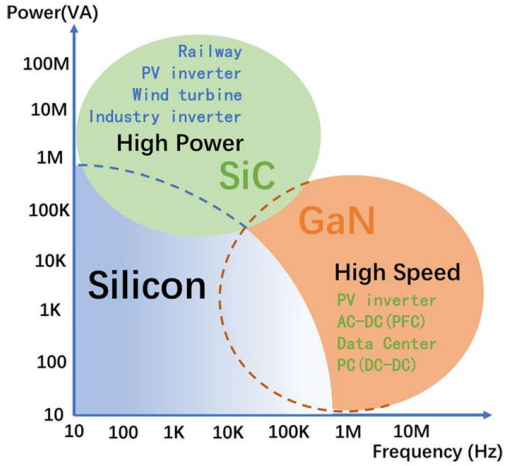
2026. 5. 14

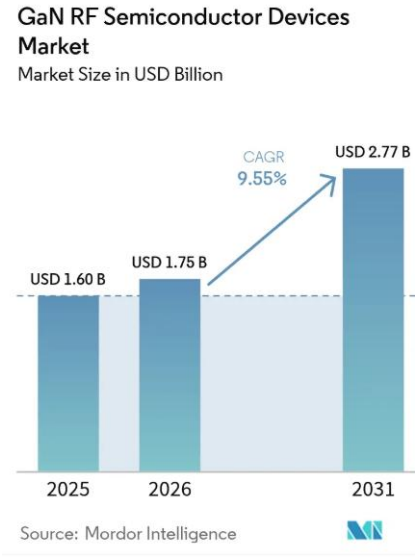
Ji-Hyeong Kim*, Il-Hwa Jeong, Se-Kyo Chung

Index

1. Introduction

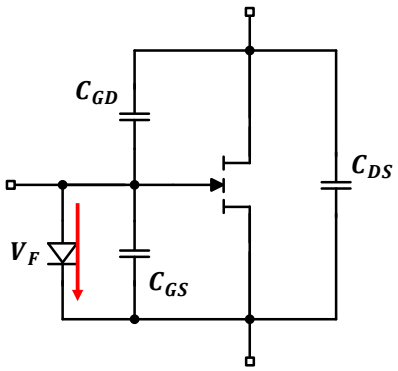
- Gallium Nitride(GaN) Semiconductor
  - Increased demand for high efficiency and high power density
  - Low switching loss, Fast switching speed





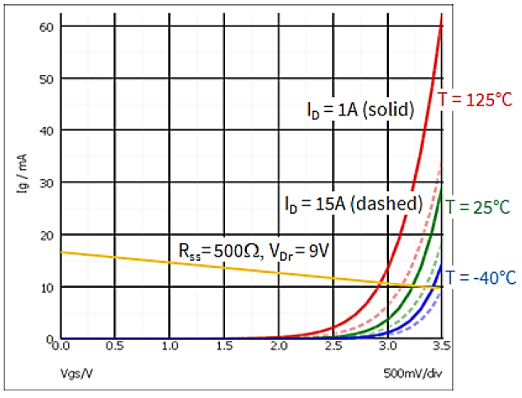
2. Background knowledge

- Gate Injection Transistor(GIT) GaN
  - non-isolated gate structure with a diode
  - provides a very reliable and robust gate structure



Rss : stegate resistanceady-state

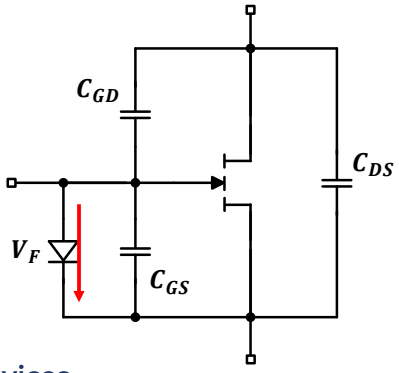
Vdr : Gate driving voltage



- Gate Diode Conduction Characteristic

Challenges of Driving GIT GaN Devices

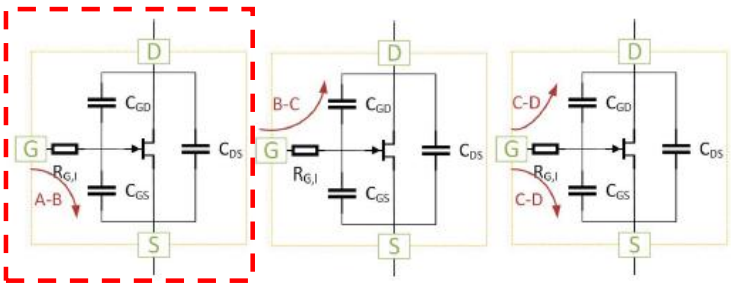
- Low Threshold Voltage
  - GIT GaN devices have a relatively low threshold voltage (Vth)
  - Negative gate voltage is required during turn-off operation

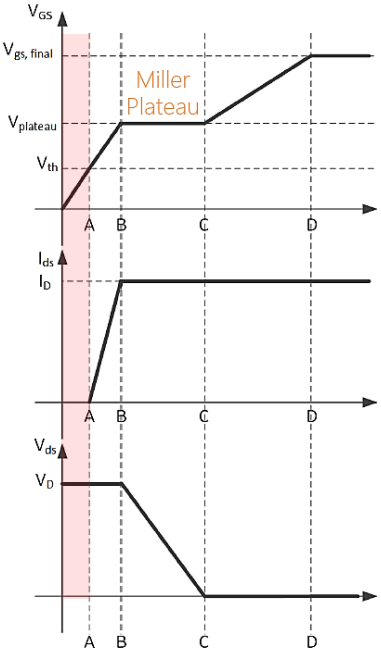


- Limitation of Conventional Gate Drivers
  - Conventional gate drivers are mainly designed for voltage-driven devices
  - Direct connection to GIT structures can cause excessive gate current

Gate driving (Turn-on)

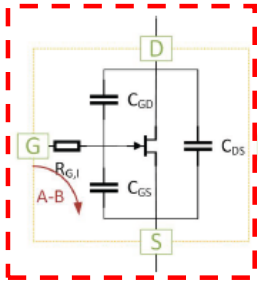
- Turn-on delay region (-A)
  - Vgs 〈 Vth
  - Most of the gate current flows through Cgs.
  - drain current and the drain voltage remain unchanged

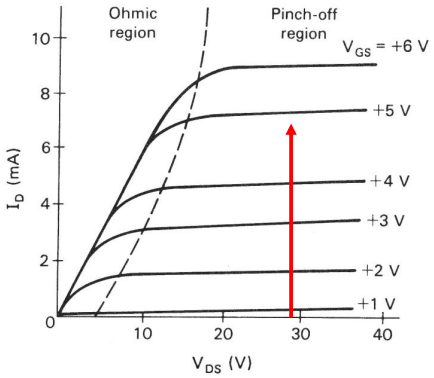


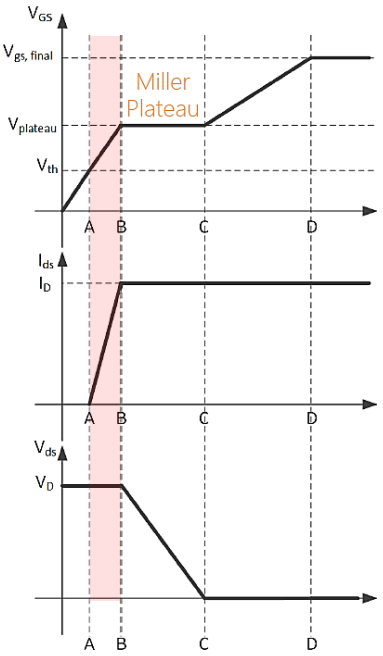


Gate driving (Turn-on)

- Current increases region (A-B)
  - Vth ⟨ Vgs ⟨ Vplateau
  - Id increases with the increase in Vgs.
  - It continues until all the current is transferred in to the MOSFET

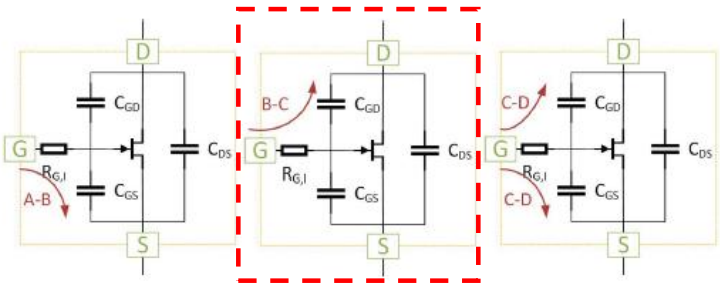


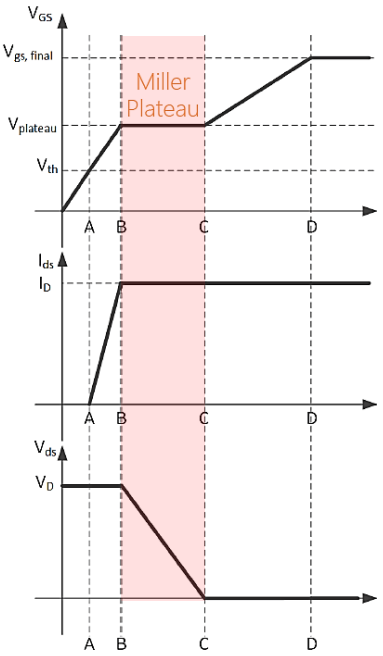




Gate driving (Turn-on)

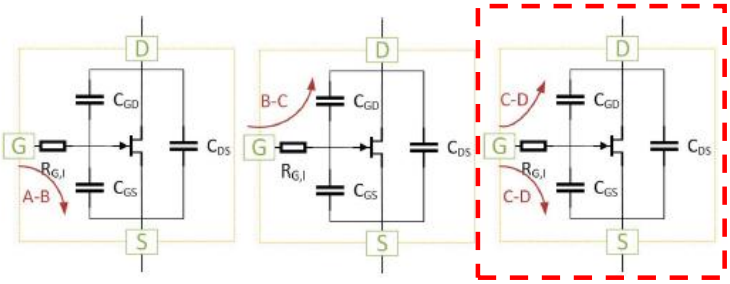
- Voltage fall region (B-C)
  - Vgs = Vplateau
  - All the gate current flows through Cgd.
  - Vgs stays steady(Miller plateau region)

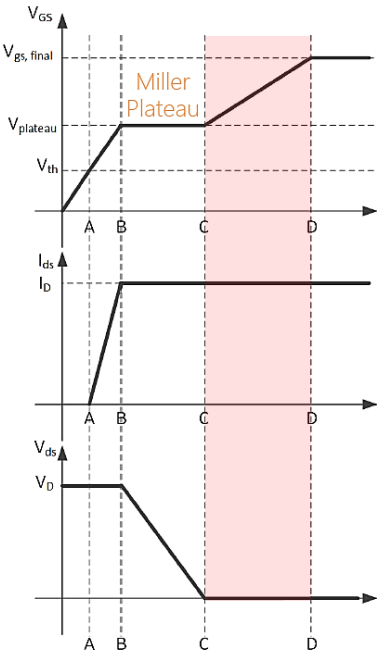




Gate driving (Turn-on)

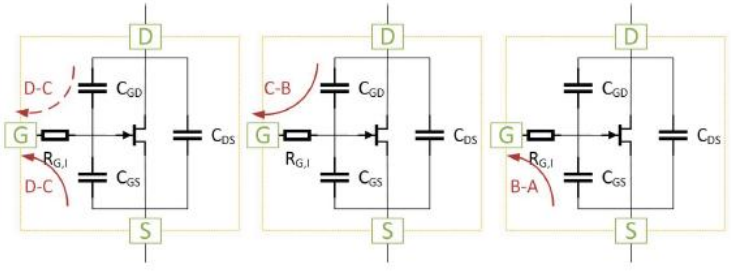
- Enhance the conducting channel region (C-D)
  - Vgs -> Vgs.final
  - Gate current is now split between the Cgd and Cgs.
  - As Vgs increases, on-resistance decreases

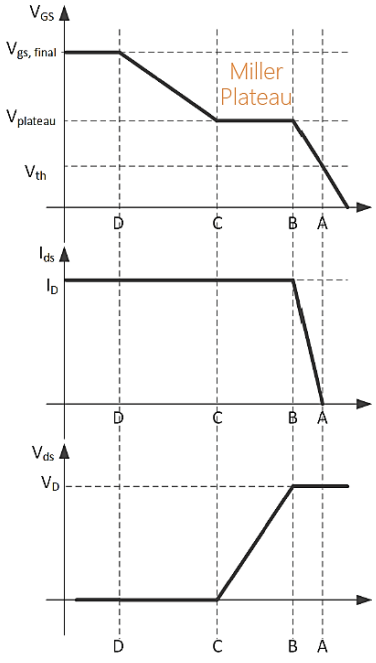




Gate driving (Turn-off)

- Turn-off transient
  - Turn-off transient fallows the reverse sequence of the turn-on process





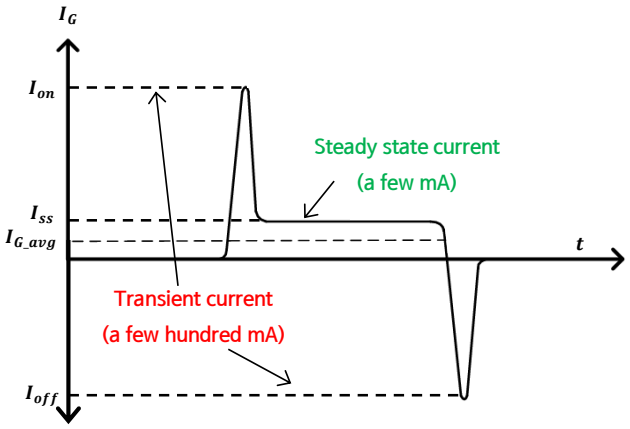
3. Gate driving circuit analysis

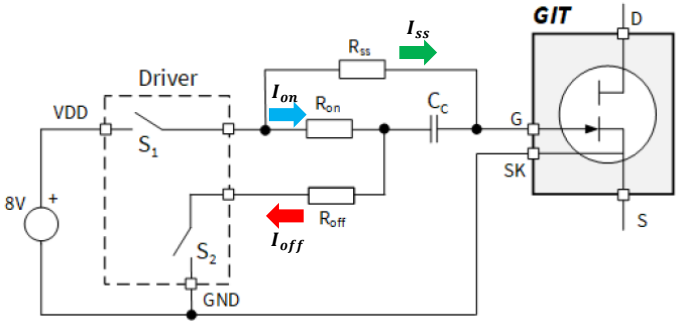
- RC interface gate driving circuit for GIT structure
  - GIT requires both a small constant gate current of a few mA and a transient current of a few hundred mA

Steady-state current path(Iss)

Turn-on transient current path(Ion)

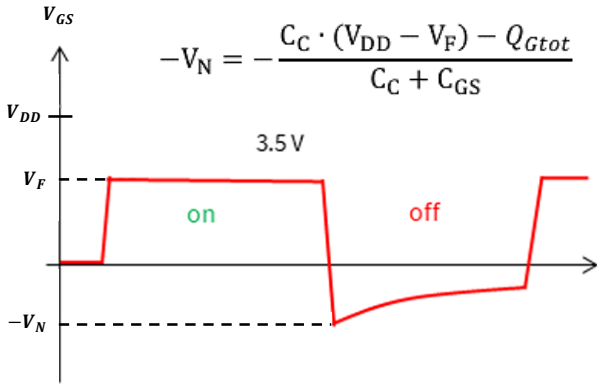
Turn-off Transient current path(Ioff)

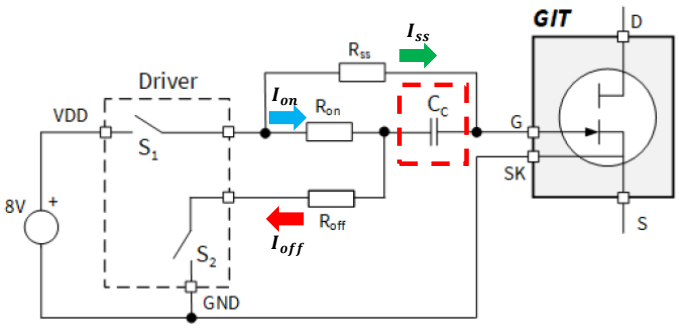




Gate driving circuit for GIT

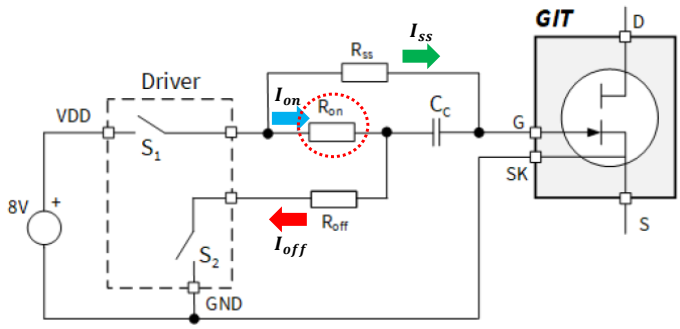
- Generates negative voltage(Vn)
  - The charge stored in Coupling capacitance(Cc) is used for reverse voltage driving during turn-off.
    - Qg : Gate charge
    - Vf : Gate diode forward voltage





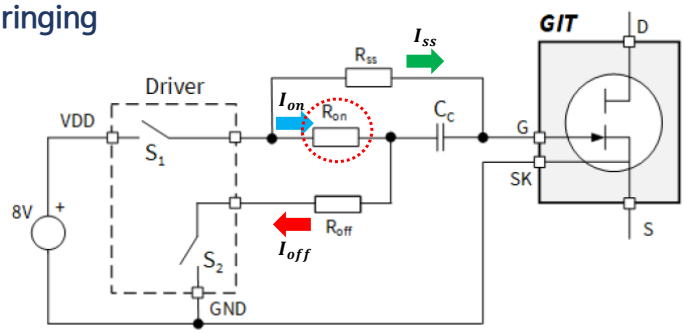
Gate drive parameter analysis and simulation

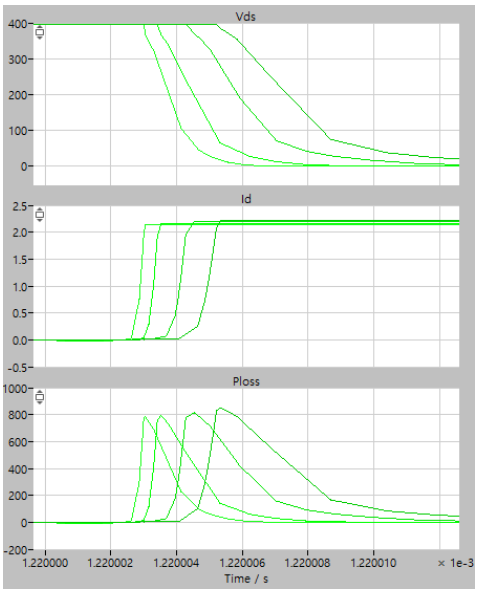
- Role of Ron
  - Controls the peak gate current during turn-on transient
  - Determines the charging speed of input capacitor(Ciss)



Gate drive parameter analysis and simulation

- Effect on turn-on switching transients (if Ron ↑)
  - As the rise in Vgs slows down, reduced Id rising slope(di/dt)
  - As the gate current discharging the Cgd decreases, reduced Vds rising slope(dv/dt)
  - Significant increase in turn-on loss Reduced voltage/current ringing

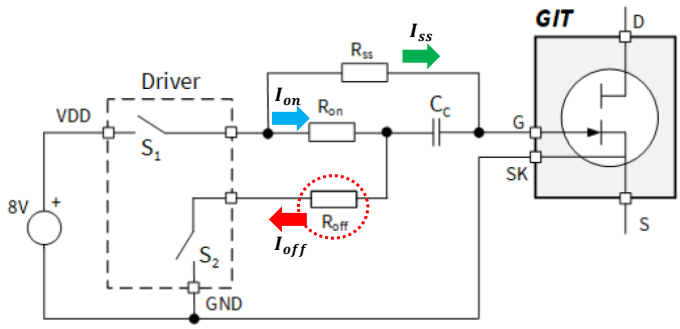




Integrated Power Electronics Lab

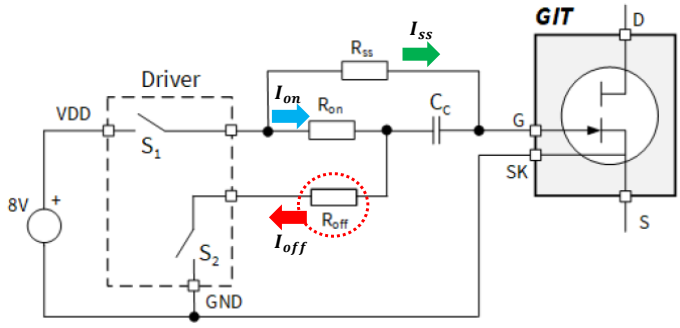
Gate drive parameter analysis and simulation

- Role of Roff
  - Directly affects the turn-off transient speed
  - Influences dv/dt, di/dt, and voltage overshoot during switching



Gate drive parameter analysis and simulation

- Effect on turn-off switching transients (if Roff ↓)
  - Larger negative peak gate current
  - The rate of increase in Vds voltage and decrease in Id current accelerates.
  - Increased voltage spike, Possible ringing

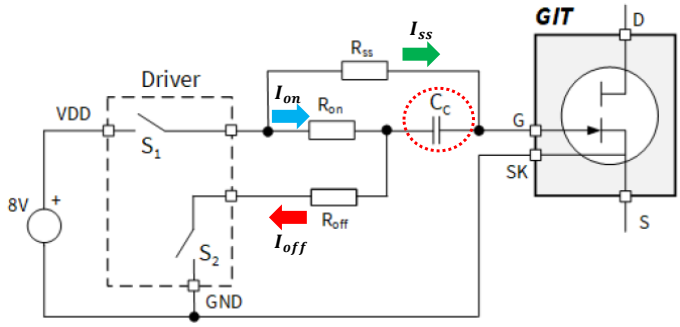


Integrated Power Electronics Lab

Gate drive parameter analysis and simulation

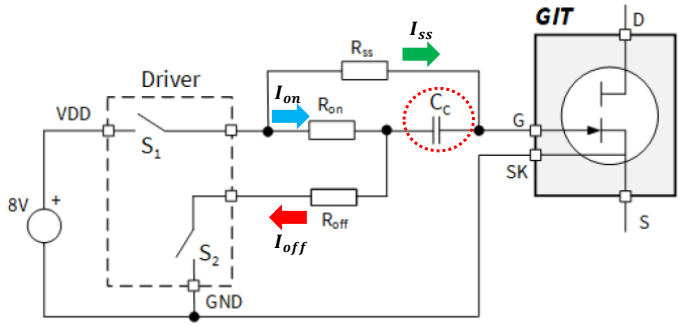
- Role of Cc
  - Stores transient gate charge during turn-on
  - Provide negative voltage during turn-off

$$C_C \geq (2 \ldots 3) \cdot Q_{Gtot}/(V_{DD} - V_F)$$



Gate drive parameter analysis and simulation

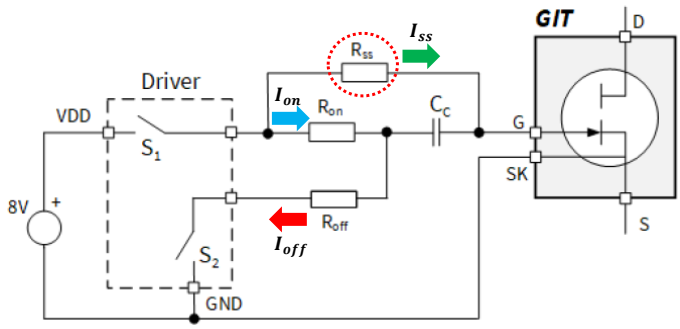
- Effect on switching transients (if Cc ↑)
  - Stronger pull-down on the gate during turn-off
  - The rate of increase in Vds voltage and decrease in Id current accelerates.



Gate drive parameter analysis and simulation

- Role of Rss
  - Determines the Rss steady-state current.
  - It has almost no effect on the transient state.

$$I_{ss} = (V_{DD} - V_F)/R_{ss}$$



4. Conclusion

- Analysis of gate driver circuits used in GIT
  - Analyzed the switching transient behavior of the RC interface gate driver for GIT GaN devices.
- Simulation Verification
  - Verified the theoretical analysis through simulation results.
  - Confirmed that each parameter has a significant effect on switching behavior and losses
- Expected Impact
  - Provides design guidelines for RC interface gate drivers in GIT GaN applications.

Q & A

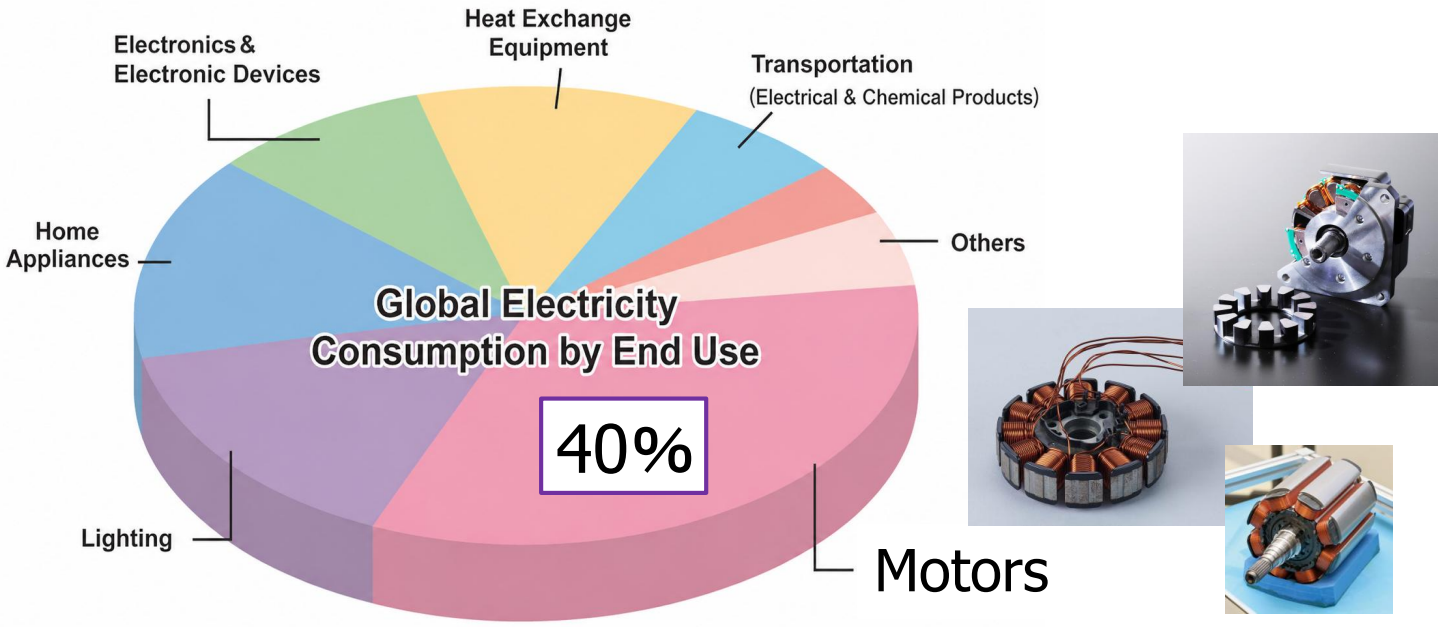
部外秘

Cogging Torque Cancellation in Axial Gap Motors Using Multiple-Wave Magnets with a Periodic Boundary Symmetric Arrangement

Asa Yamauchi*, Wataru Kitagawa
Nagoya Institute of Technology
May 14, 2026

Outline

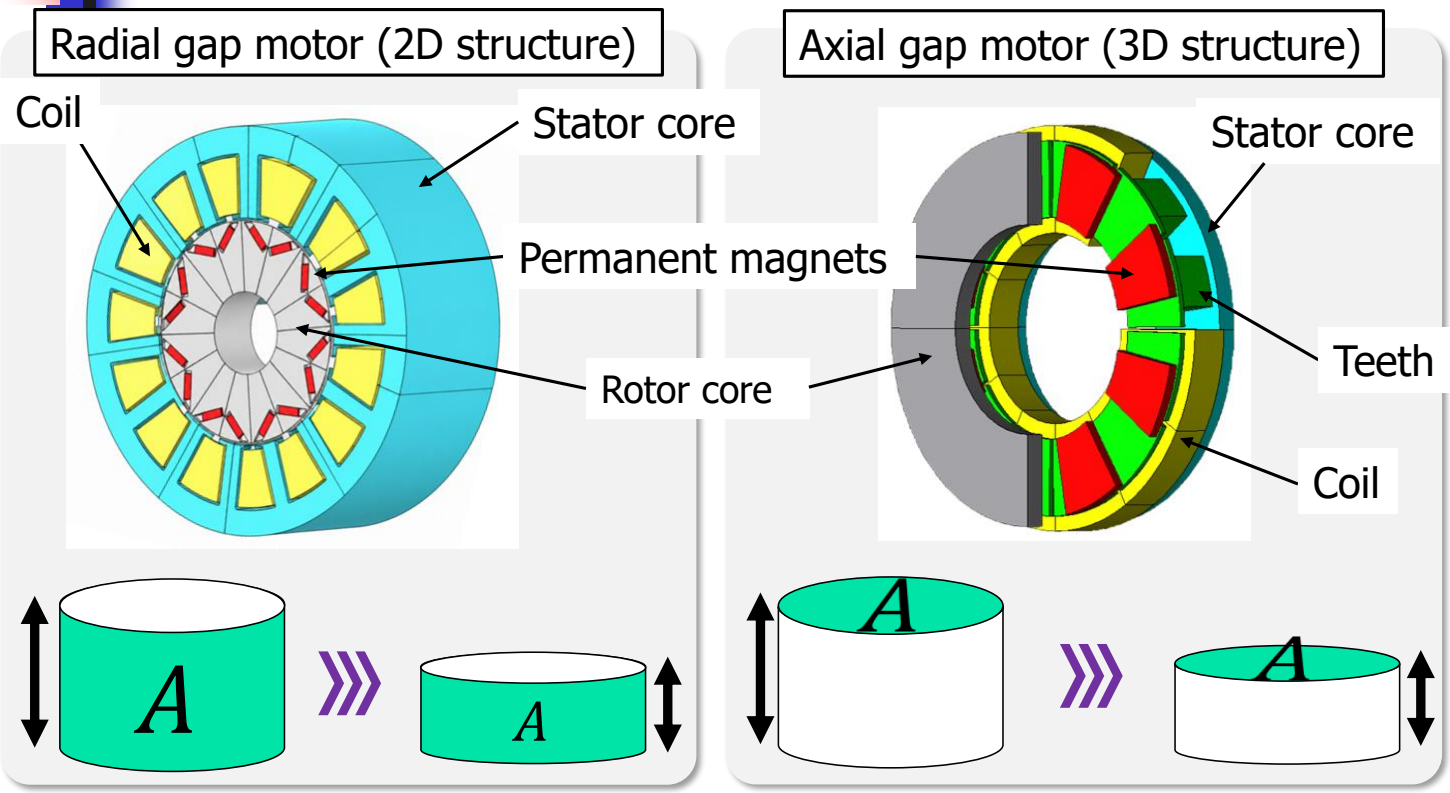
Research Background



Motor Systems（Motor Summit 2008）

The demand for high-efficiency motors is increasing.

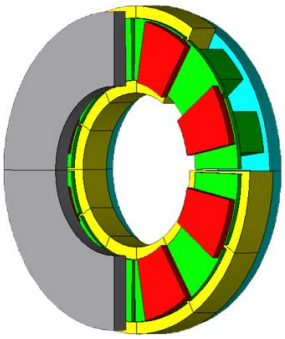
Axial Gap Motors



$$T \propto B \cdot A \cdot r$$

(B:Magnetic flux density, A:The area facing magnets and stator core, r:Effective radius)

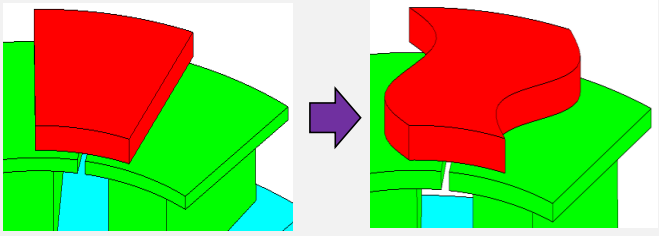
Research Purpose



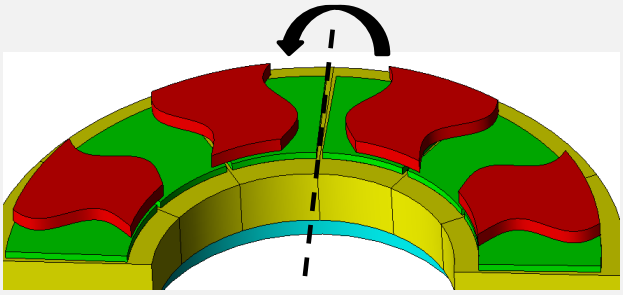
Problem

Cogging torque and torque ripple are likely to occur, leading to uncomfortable vibrations and oscillations.

① Magnet shape



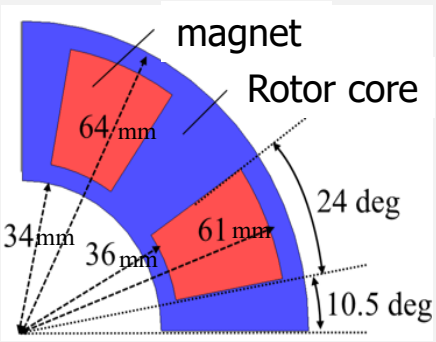
② Magnet arrangement



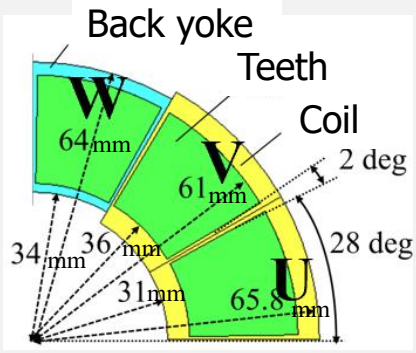
Cancel the harmonic components to reduce cogging torque.

Proposed Motor

Rotor core



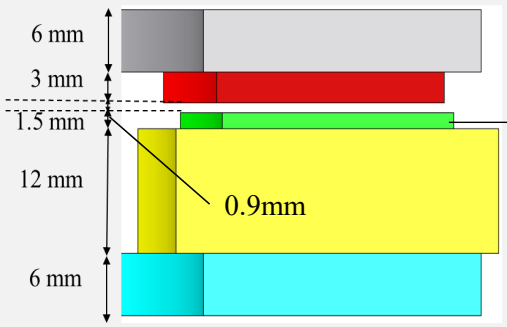
Stator core

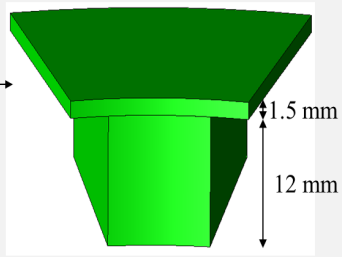


Analysis specification

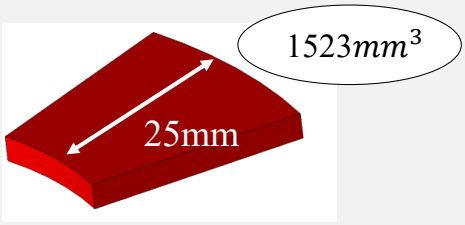
magnet	N50M
Magnet temperature [deg]	20
Residual flux density [T]	1.415
Magnetization	Parallel
Core Material	35JN300
Number of rotations [rpm]	4000
Rated current [A]	70.5
Current frequency [Hz]	266.7
Air gap [mm]	0.9

Motor size





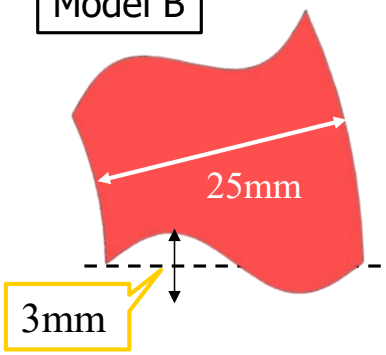
Teeth



Magnet

Proposed Motor : Magnet Shape

Model B



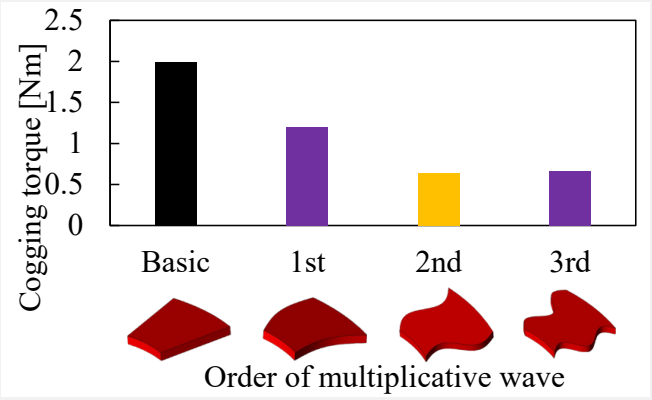
Side waveform of magnet

$$f(x) = 3 \times \sin\frac{2\pi x}{25}$$

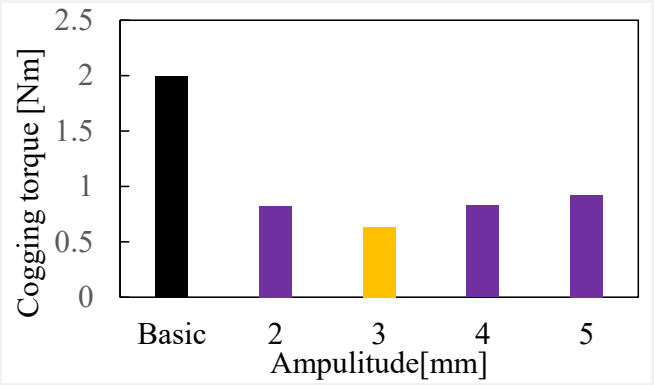
Amplitude

Sin waveform with a period of 25mm

Waveform order

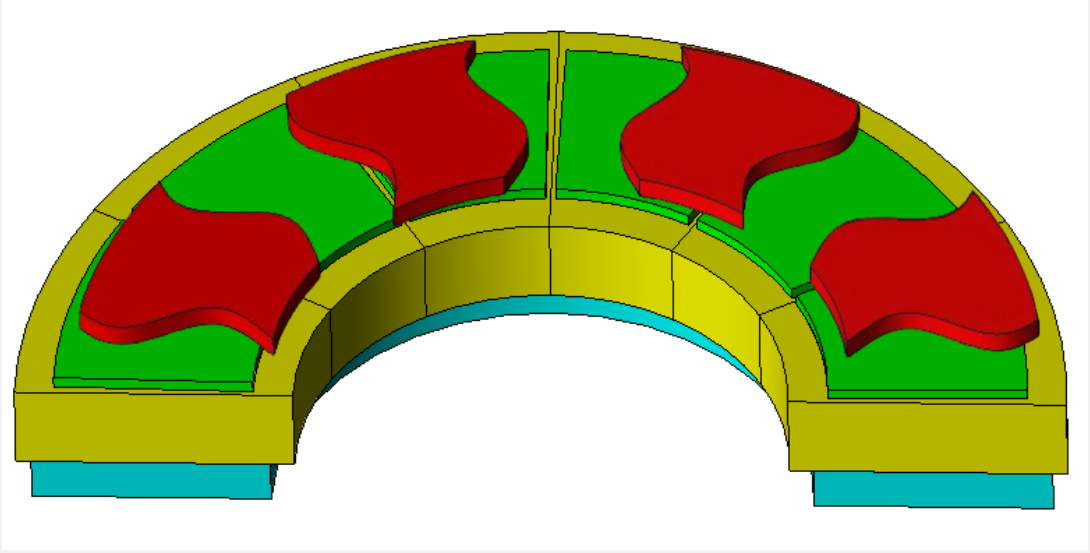


Waveform order



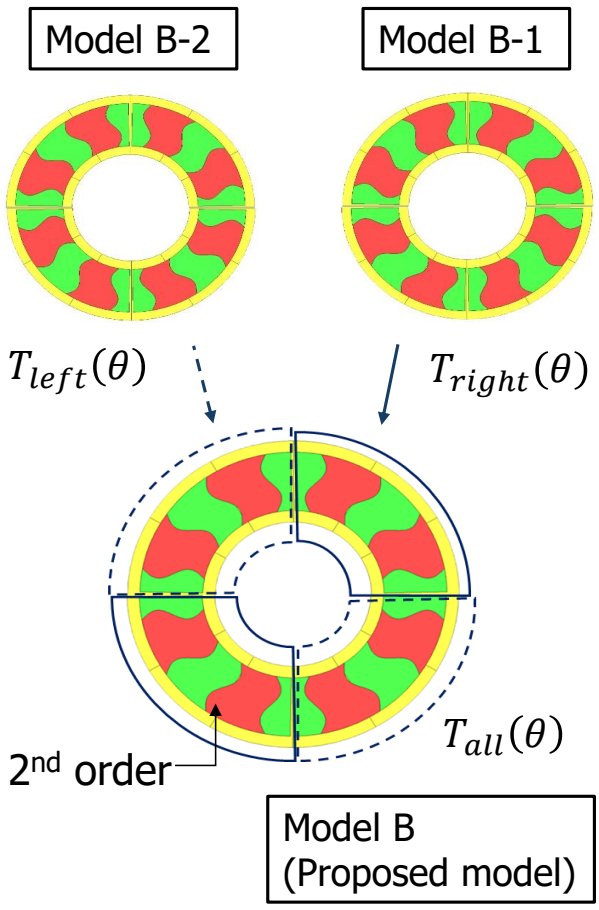
Proposed Motor : Magnet Arrangement

½ of model B

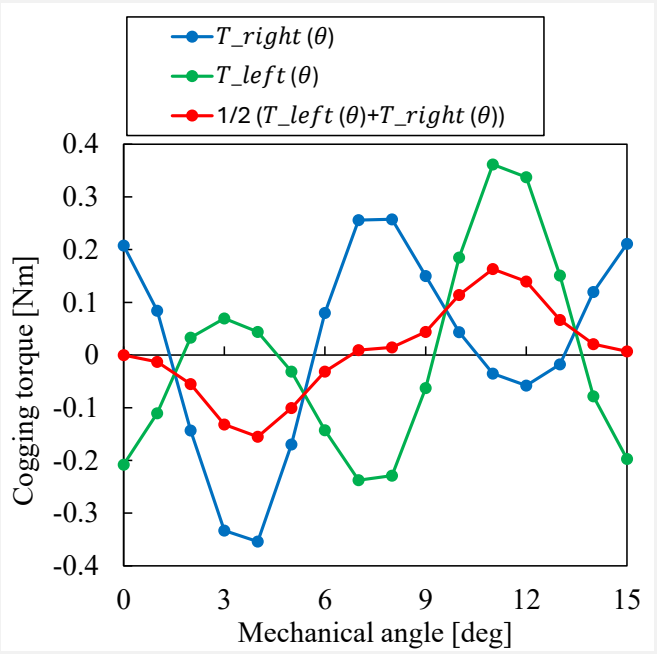


The magnets are arranged to be line-symmetric with respect to the 90-degree periodic boundary.

Proposed Motor : Magnet Arrangement



Expected cogging torque



$$T_{all}(\theta) \approx \frac{1}{2}\left(T_{left}(\theta) + T_{right}(\theta)\right)$$

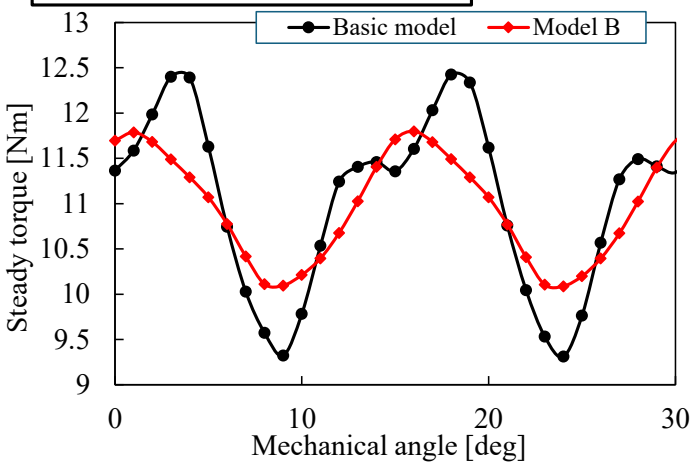
Evaluation Items

1. Average torque T_{ave}
2. Torque ripple $T_{rip}=T_{max} - T_{min}$
3. Cogging torque $T_{cog} = T_{max\_cog} - T_{min\_cog}$

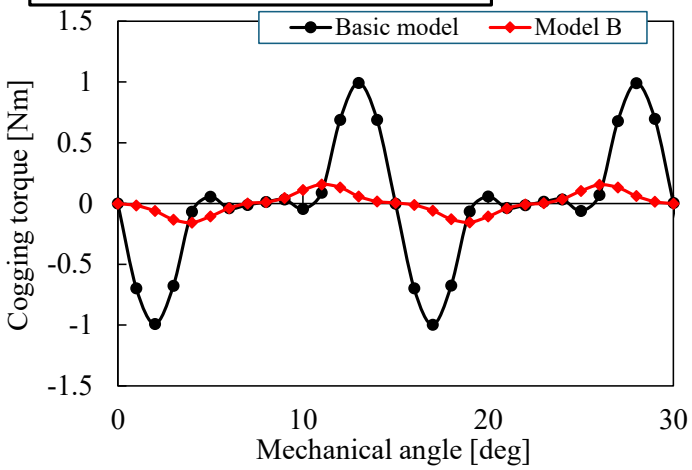
T_{ave} : Average torque
T_{max} : Maximum torque
T_{min} : Minimum torque
T_{max_cog} : Maximum cogging torque
T_{min_cog} : Minimum cogging torque

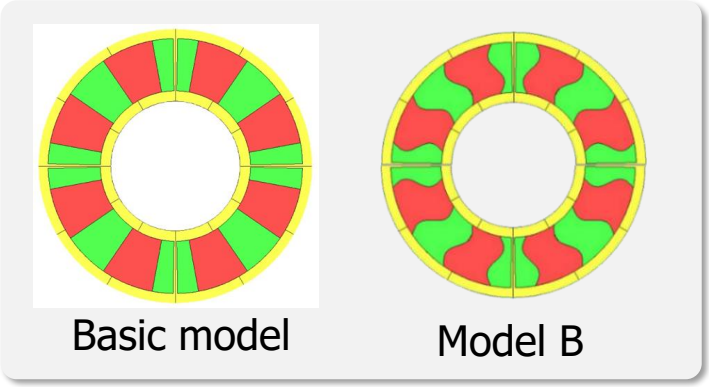
Result : Motor Characteristics

Steady torque waveform



Cogging torque waveform





Motor characteristics

	Average torque [Nm]	Torque ripple [Nm]	Cogging torque [Nm]
Basic model	11.04	3.14	1.99
Model B	10.95 (-0.82%)	1.71 (-45.54%)	0.32 (-83.92%)

Deterioration　Improvement

FFT Analysis

The waveform of the cogging torque can be expressed by the following approximate equation.

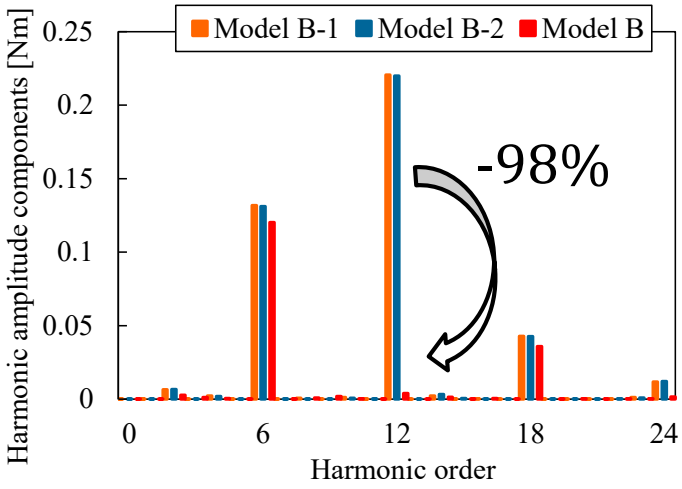
$$T(\theta) = \sum_{t=0}^{\frac{N}{2}} A_t \cos\left(2\pi t \frac{\theta}{N} + \phi_t\right)$$

t:Harmonic order
A_t[Nm]: Amplitude component of the t−th harmonic
ϕ_t[rad]: Phase component of the t-th harmonic
θ[deg]:Mechanical angle
N:Number of data points used for FFT analysis

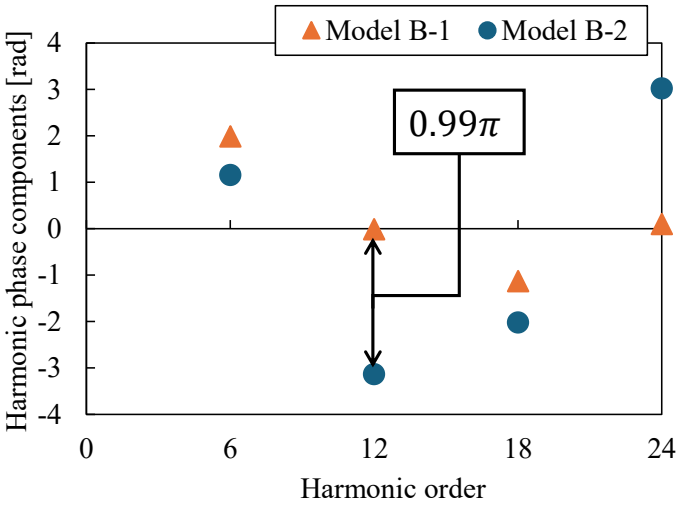
In this study, the analysis was conducted over one electrical cycle (360 electrical degrees = 90 mechanical degrees); therefore, the number of data points used for the FFT analysis is N=90.

Result : FFT Analysis

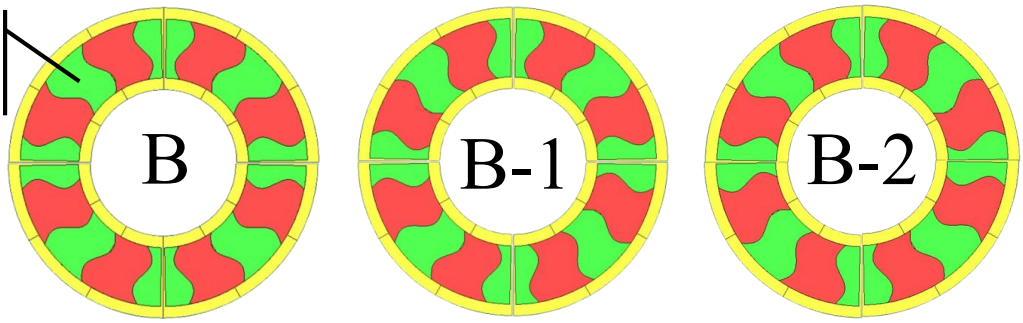
Harmonic amplitude



Harmonic phase

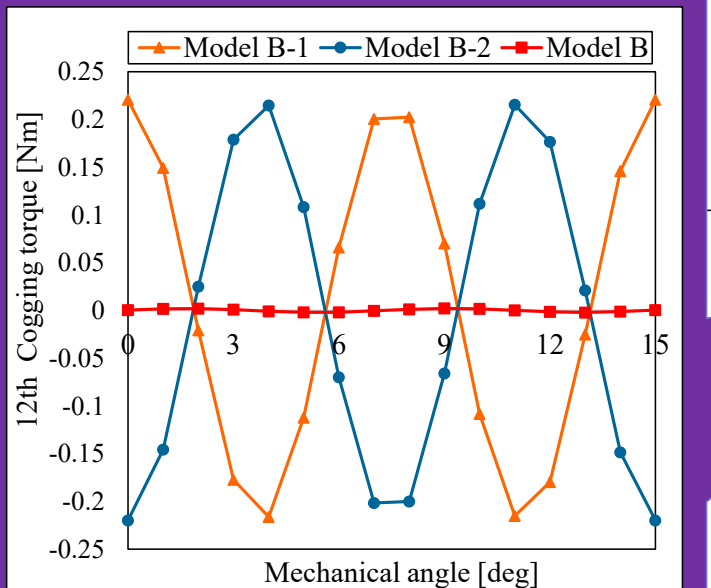


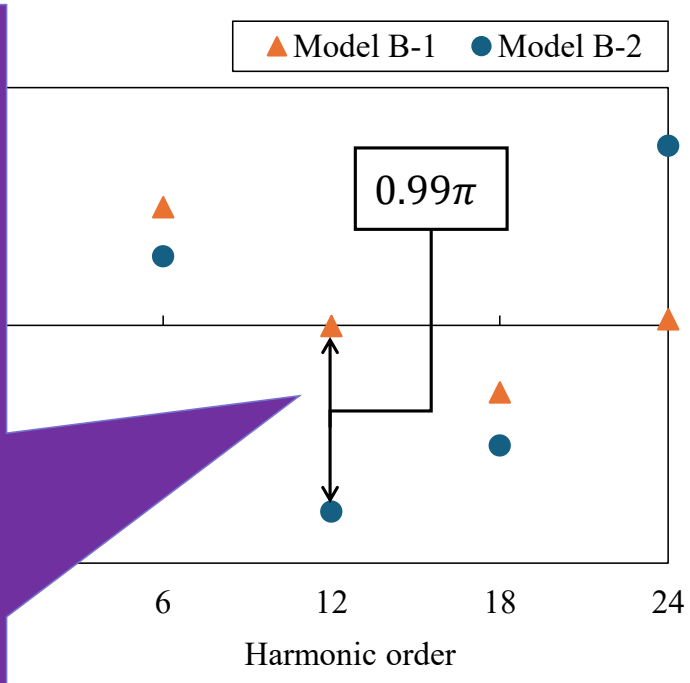
Proposed model



Result : FFT Analysis

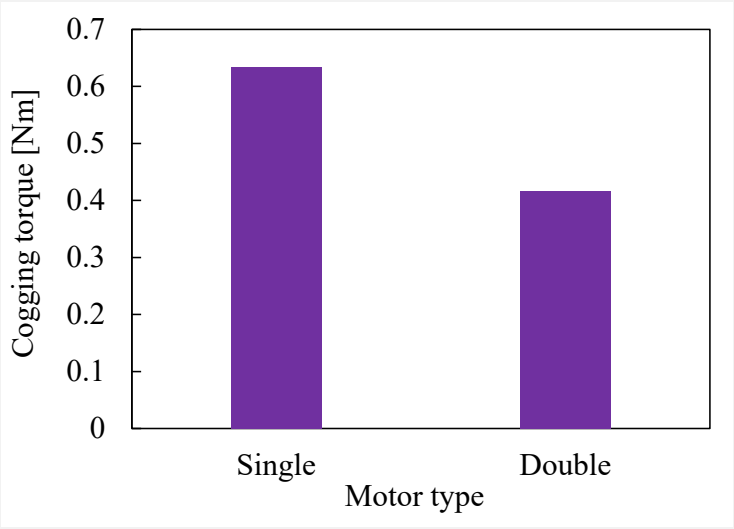
12th harmonic waveform

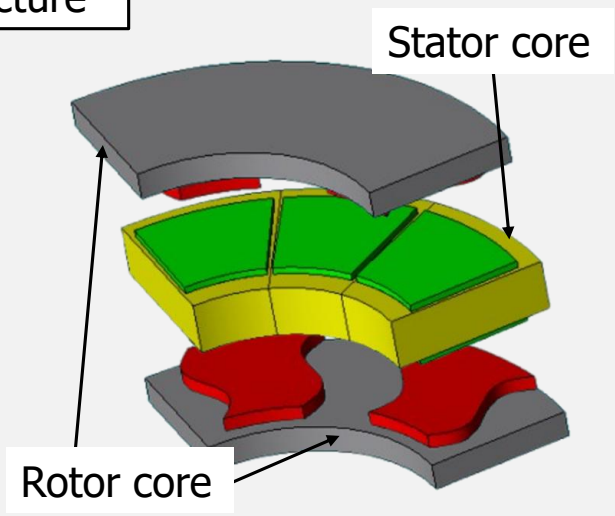




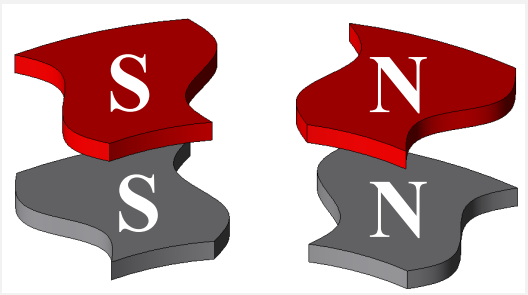
Development into a Double Structure

Cogging reduction effect by double structure





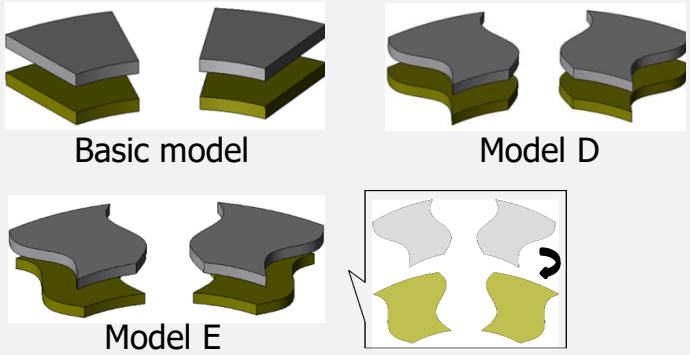
Turn around



先行研究：佐藤大祐，水野暁斗，北川亘，竹下隆晴，
“ダブルアキシャルギャップモータのコギングトルク相殺可能な磁石形状設計手法の検討”，
日本AEM学会誌，Vol. 32(2)，pp.300-305，2024.

Development into a Double Structure

Magnet arrangement

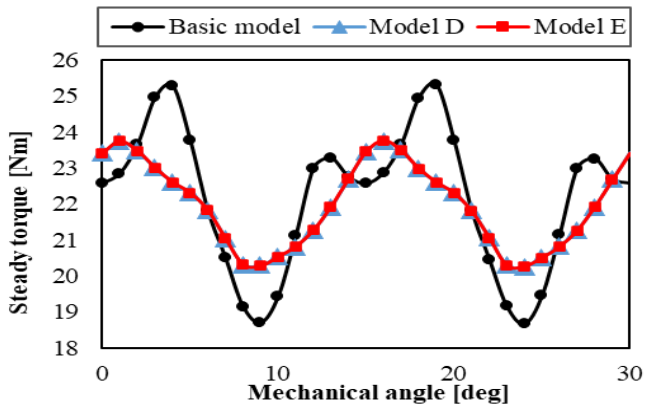


Motor characteristics

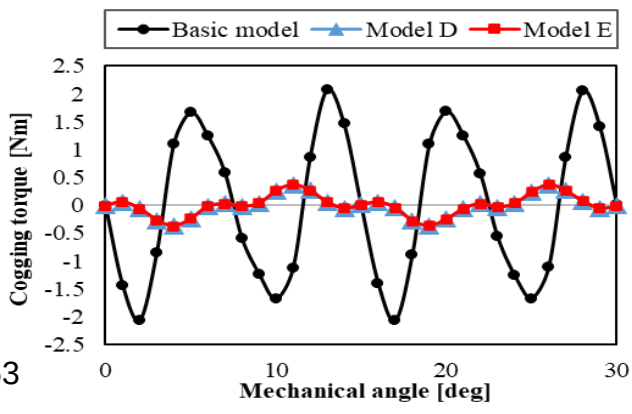
	Average torque [Nm]	Torque ripple [Nm]	Cogging torque [Nm]
Basic model	22.20	6.66	4.15
Model D	22.20 (±0%)	3.51 (-47.30%)	0.75 (-81.93%)
Model E	22.00 (-0.90%)	3.50 (-47.45%)	0.76 (-81.69%)

Deterioration　Improvement

Steady torque waveform



Cogging torque waveform



Conclusion

Research purpose

Reduction of cogging torque by magnet arrangement

Result

Average torque: decreased by 0.82%
Cogging torque: improved by 83.92%
Torque ripple: improved by 45.54%

Future work

Design of a double axial-gap motor for reducing cogging torque through the cancellation effect of the upper and lower magnet arrangements.

An Improved PWM Technique of Three_Phase Motor Drives for Common Mode Voltage Reduction

2026. 5. 13

Yunho Ha

Index

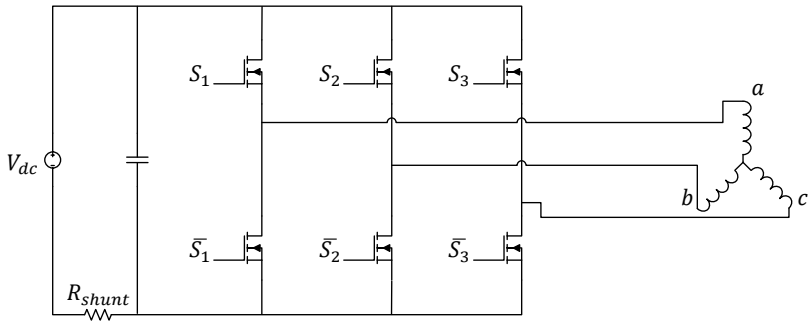
1. Introduction

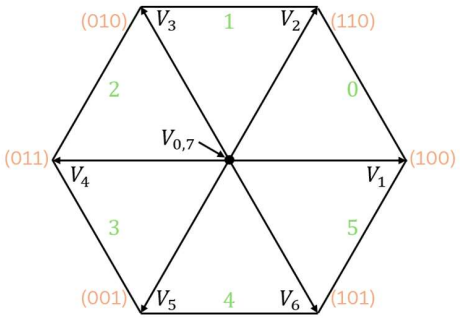
- Research Background
  - Miniaturization and efficiency of the system ← High-speed switching of switch elements
  - EMI and CMV issues need to be resolved
  - Must be compatible with 1-shunt inverter systems

- Proposed solution
  - Solve the problem with just a software change
  - Improved PWM available for 1-shunt inverters

2. Conventional Algorism

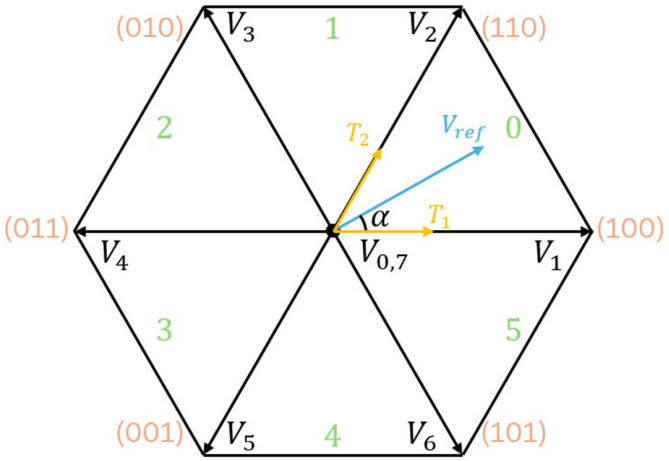
- Three-Phase, two-level voltage source 1-shunt inverter
  - Active Voltage Vector : $V1 \sim V6$
  - Zero Voltage Vector : $V0, V7$





2. Conventional Algorism

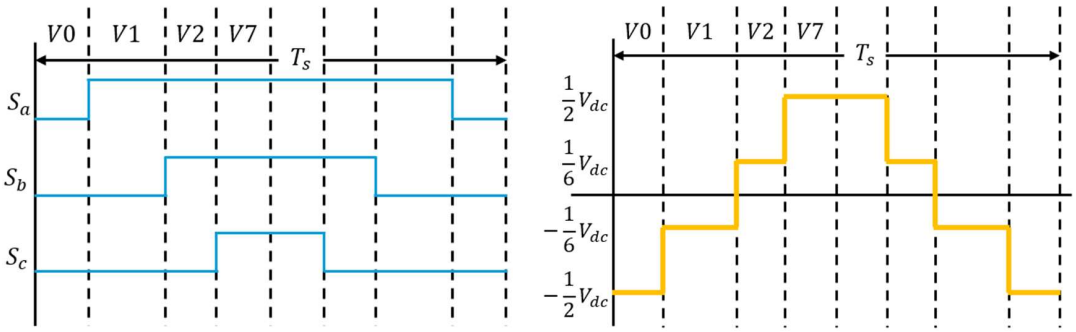
- MI(Modulation Index)
  - A method to systematize and utilize the magnitude of voltage output
  - $m_i = \frac{V_{1peak}}{V_{dc}/2}$
  - V_{1peak} : Magnitude of the fundamental wave



- CSVPWM(Conventional Space Vector PWM)
  - $T_1 = \frac{2\sqrt{3}}{\pi} M_i sin(60° - \alpha) T_s$
  - $T_2 = \frac{2\sqrt{3}}{\pi} M_i sin(\alpha) T_s$
  - $T_0 = T_s - T_1 - T_2$

2. Conventional Algorism

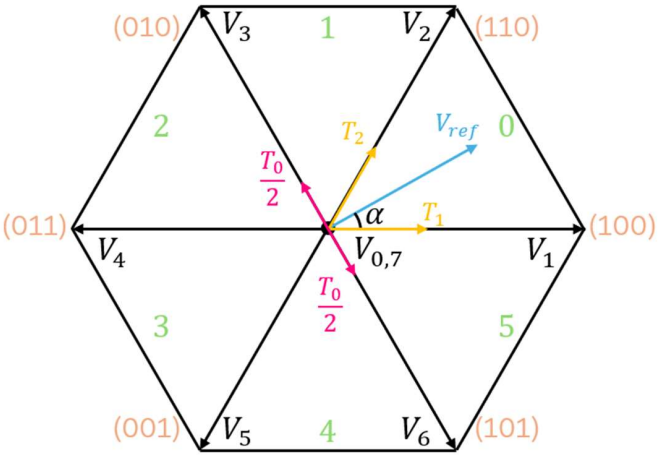
- CSVPWM CMV(Common Mode Voltage)
  - $\Delta CMV = V_{dc}$
  - Number of Changes per switching cycle : 6



Sector 0

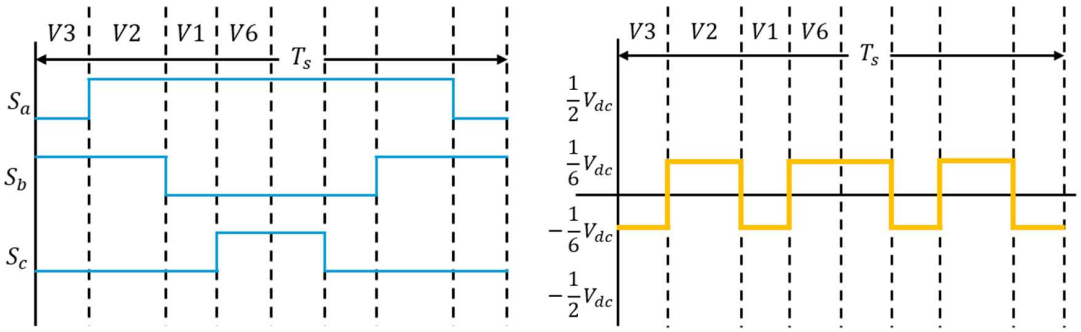
2. Conventional Algorism

- CAZSPWM
  - Zero voltage vector -〉 Use two opposite active voltage vectors
  - $T_1 = \frac{2\sqrt{3}}{\pi} M_i sin(60° - \alpha) T_s$
  - $T_2 = \frac{2\sqrt{3}}{\pi} M_i sin(\alpha) T_s$
  - $T_0 = T_s - T_1 - T_2$
  - But, CAZSPWM Can't use at 1-shunt Inverter



2. Conventional Algorism

- CAZSPWM CMV
  - $\Delta CMV = \frac{V_{dc}}{3}$
  - Number of Changes per switching cycle : 6

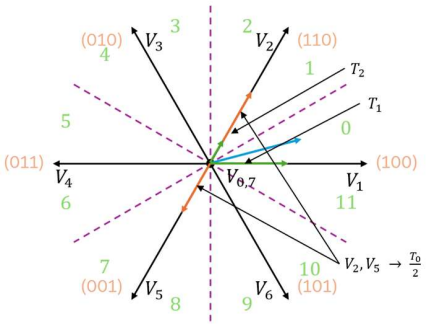


Sector 0

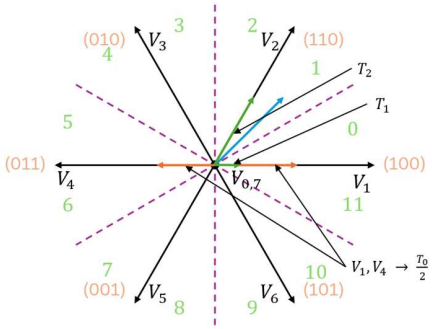
3. Proposed PWM

- Proposed AZSPWM can using 1-shunt inverter
  - Divide the sector into 12 sections at a 30-degree angle.
  - Case 1, Sector 0, 3, 4, 7, 8, 11 : Using vector for active zero V(N+2), V(N+5)
  - Case 2, Sector 1, 2, 5, 6, 9, 10 : Using vector for active zero V(N+1), V(N+4)

  * N : Sector number at CSVPWM



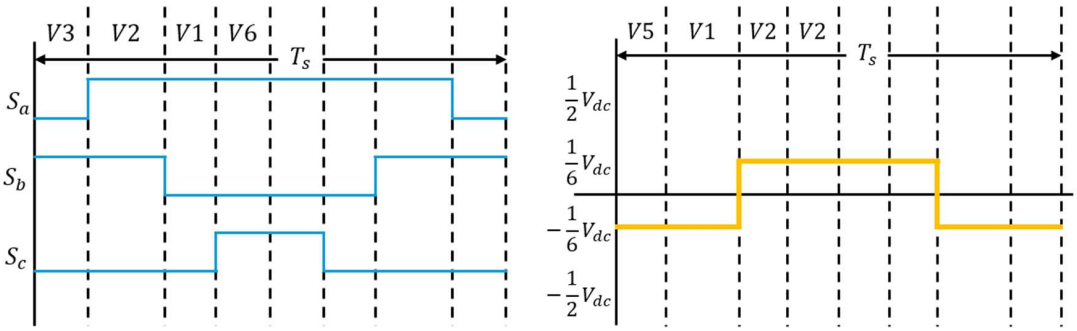
Case 1



Case 2

3. Proposed PWM

- Proposed CAZSPWM CMV
  - $\Delta \boldsymbol{CMV} = \frac{V_{dc}}{3}$
  - Number of Changes per switching cycle : 2

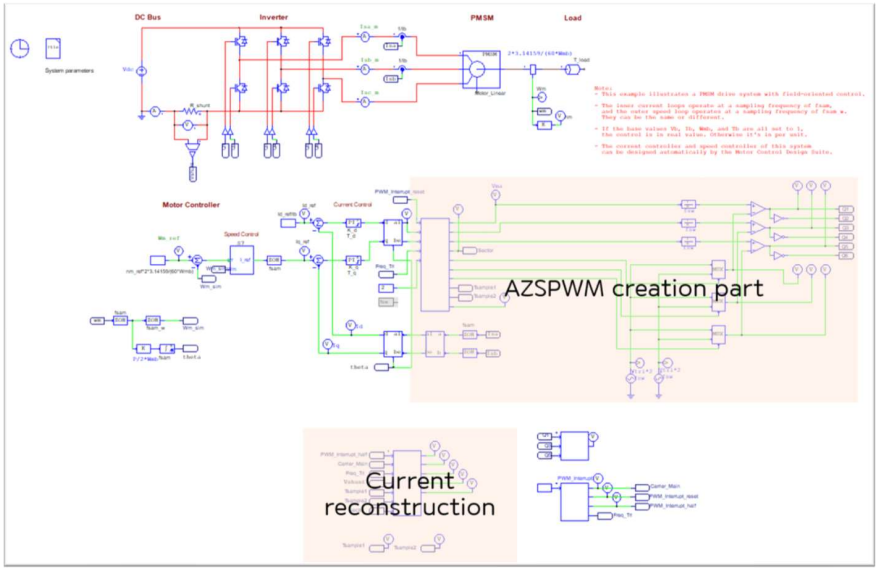


Sector 0

Integrated Power Electronics Lab

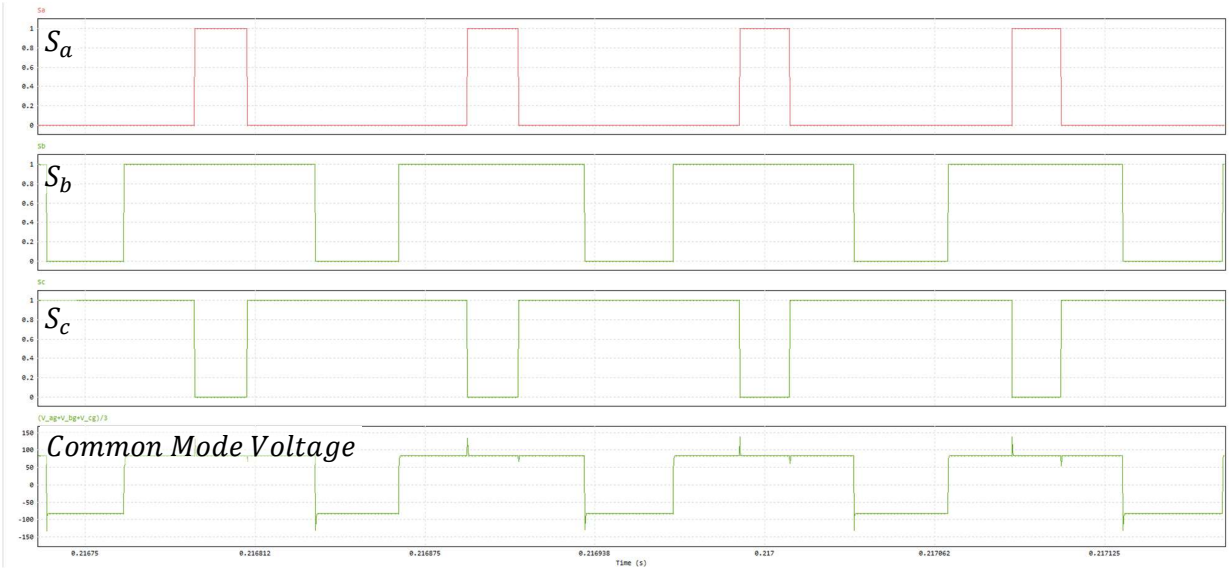
4. Simulation

- Circuit



4. Simulation

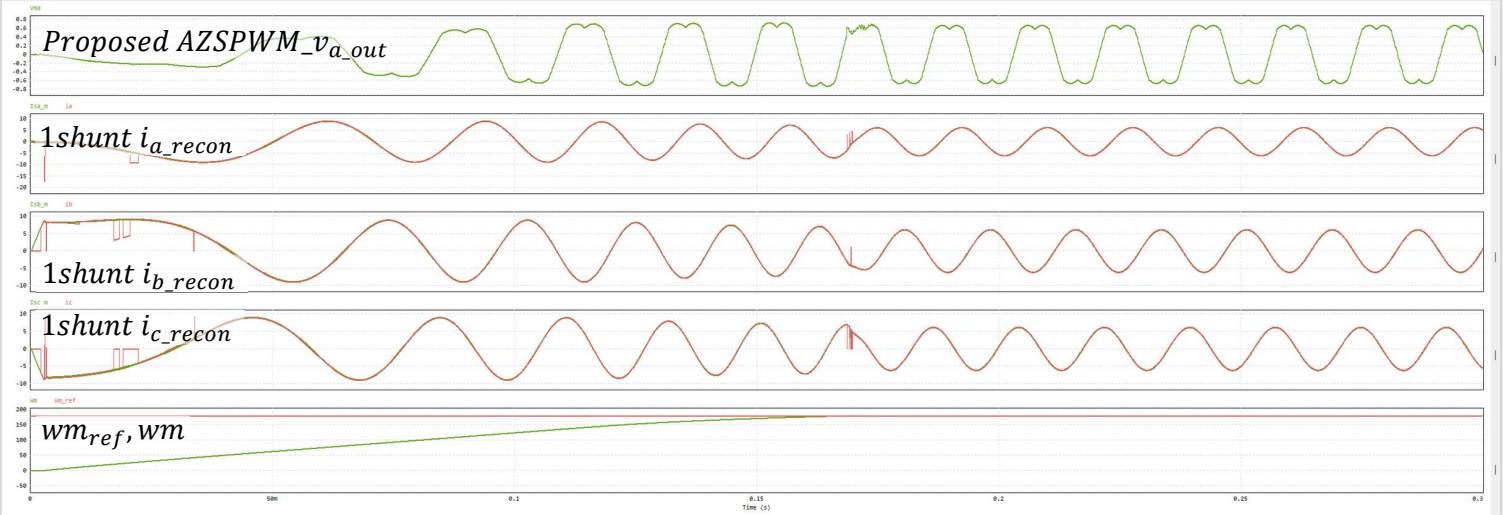
- Common Mode Voltage waveform



Integrated Power Electronics Lab

4. Simulation

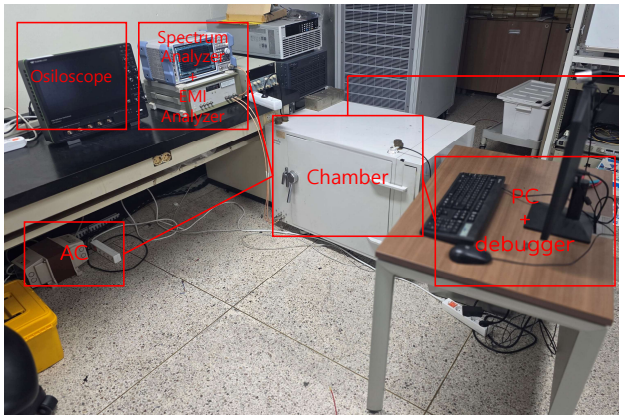
- Current reconstruction waveform



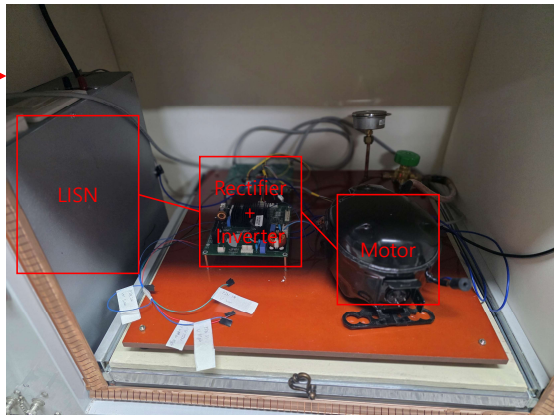
5. Experiment

- Environment

Outerior

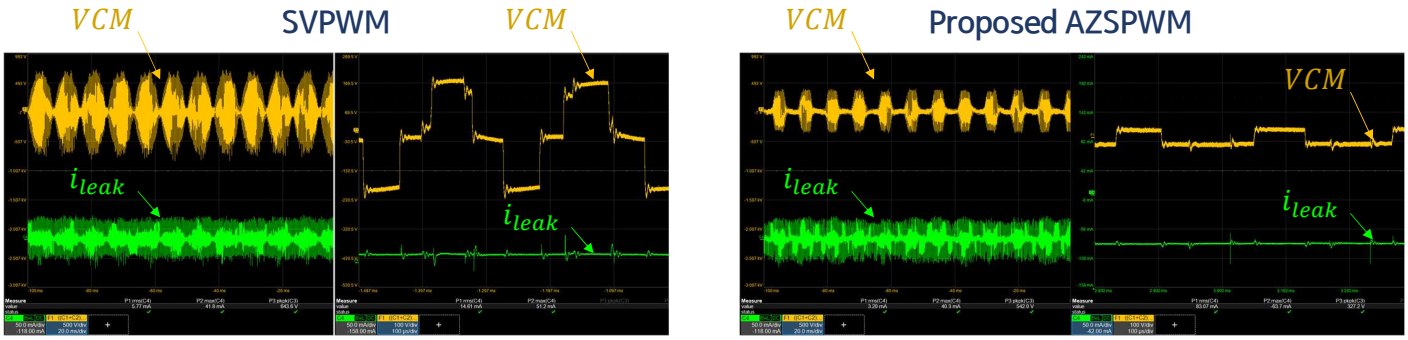


Chamber interior



5. Experiment

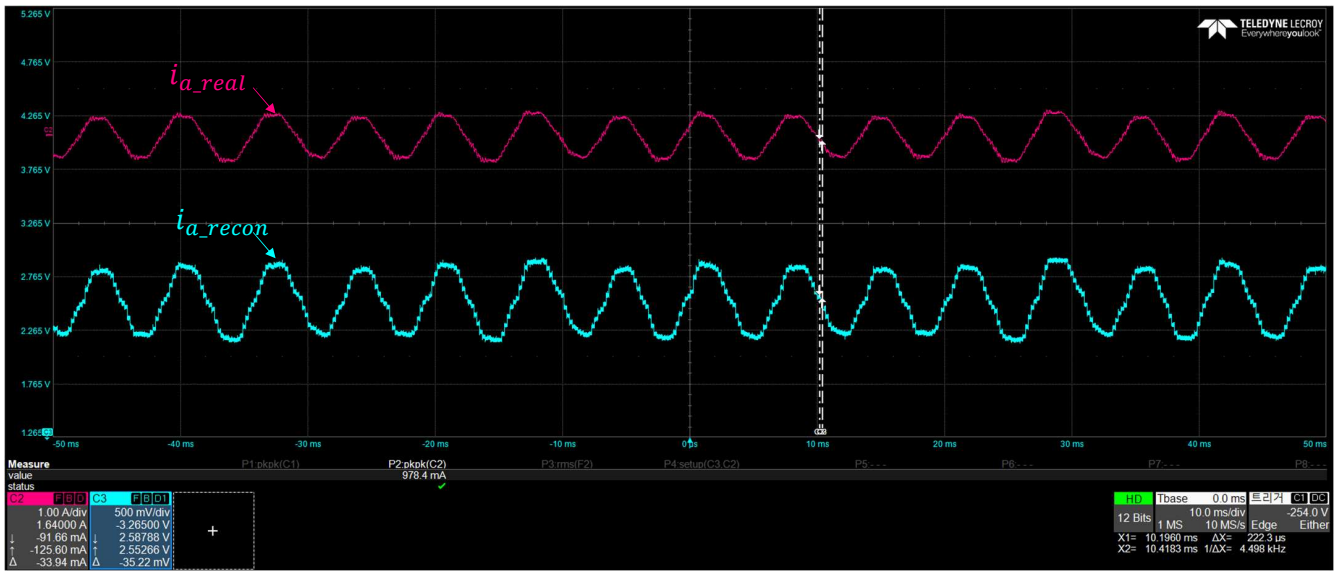
- VCM, Leakage Current SVPWM and Proposed AZSPWM Waveform



	SVPWM	Proposed AZSPWM
ΔVCM	500 [V]	166 [V]
i_{leak}	5.77 [mA]	3.2 [mA]

5. Experiment

- Current reconstruction waveform



Integrated Power Electronics Lab

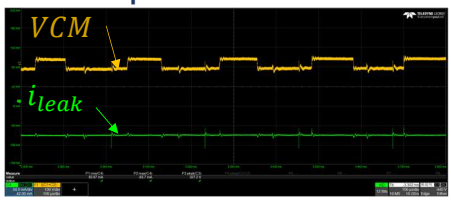
6. Conclusion

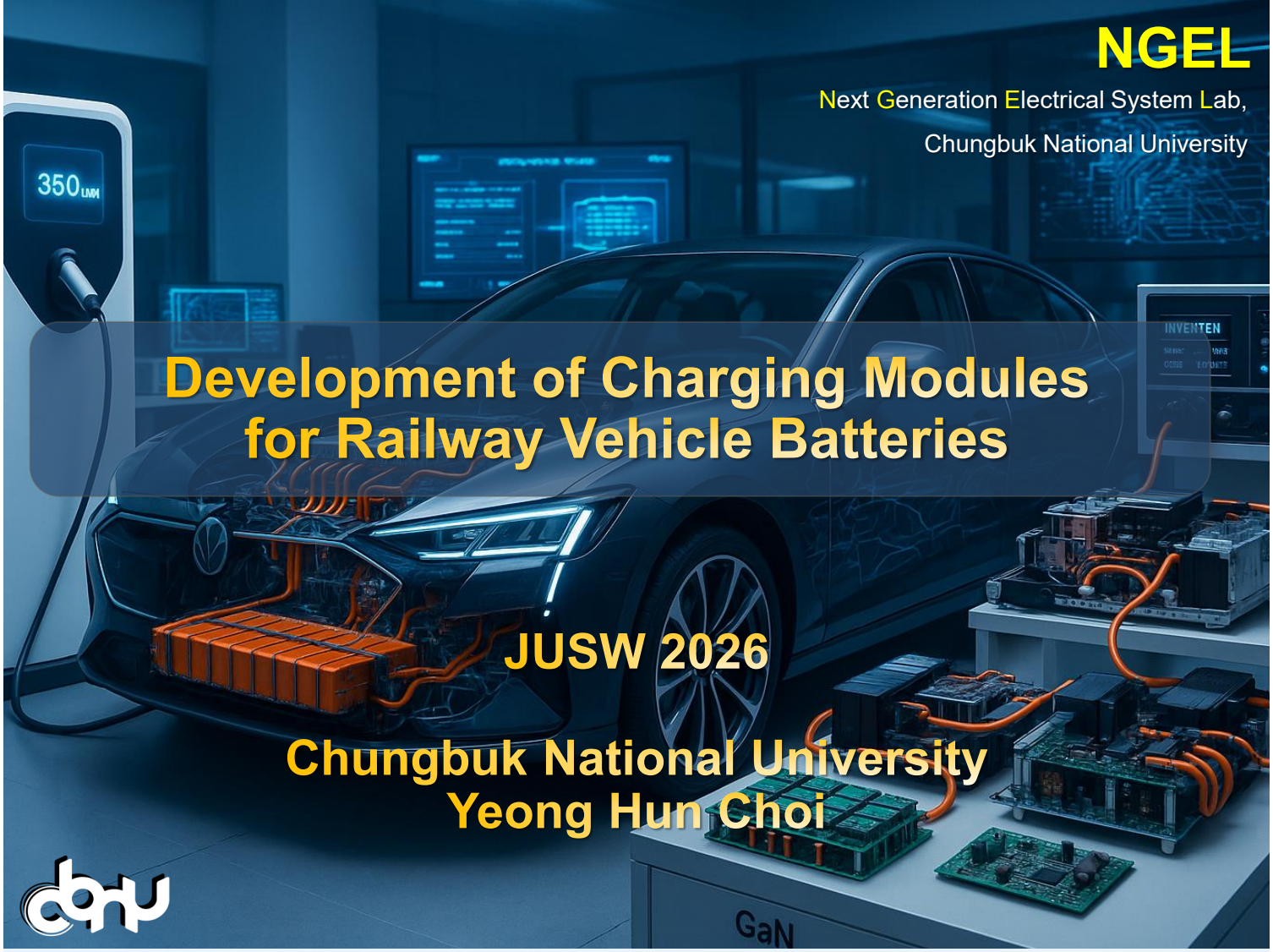
- Summation
  - Proposal of an AZSPWM technique usable in 1-shunt inverters
  - Verification through simulation and experiment

	CSVPWM	CAZSPWM	Proposed AZSPWM
ΔCMV	V_{dc}	$V_{dc}/3$	$V_{dc}/3$
CMV change time Per switching cycle	6	6	2
i_{leak}	5.77 [mA]	-	3.2 [mA]

SVPWM

Proposed AZSPWM





Development of Charging Modules for Railway Vehicle Batteries

JUSW 2026

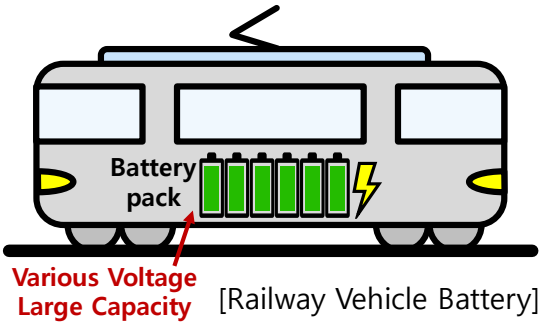
Chungbuk National University
Yeong Hun Choi

Contents

Battery Charging Modules

❑ Railway Battery

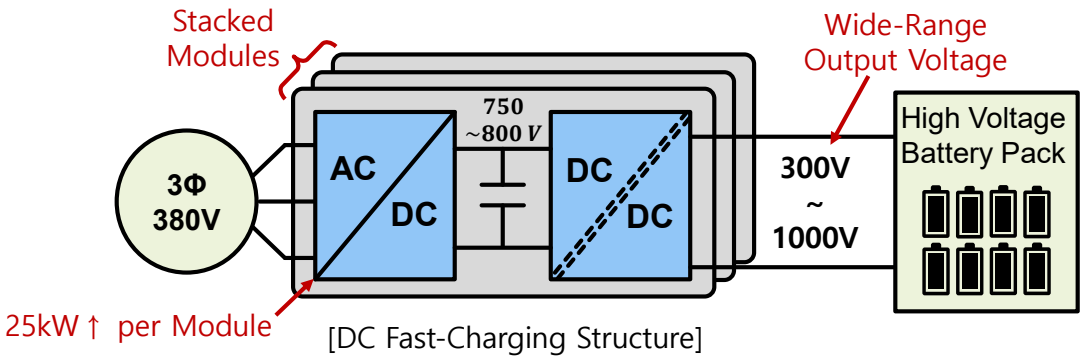
- Railway battery voltage varies depending on vehicle type, battery configuration and state of charge (SOC)
- A wide output voltage range is required for charging various battery packs
- High-power charging is required to reduce charging time for large-capacity batteries



[Railway Vehicle Battery]

❑ Structure of DC Fast Charging Modules

- 2-stage structure with a 3-phase AC/DC converter and an isolated DC/DC converter
  - AC/DC : Rectification, Voltage boosting, Power factor correction
  - DC/DC : Galvanic isolation, CC/CV charging control



[DC Fast-Charging Structure]

AC/DC Converter Topology

❑ AC/DC PFC Topology Comparison

	2-Level	3-Level NPC	3-Level Vienna	3-Level TNPC	3-Level ANPC
Current THD	High	Low	Low	Low	Low
Voltage stress	High	Low	Low	Low	Lowest
Power density	Low	Higher	High	High	Higher
Bidirectional	Yes	Yes	No	Yes	Yes
Efficiency	Low	High	High	High	Highest
Cost	Low	High	Mid	Mid	High
Control	Easy	Mid	Mid	Mid	Mild
Input inductor size	Large	Low	Low	Low	Low

[Topology comparison of AC/DC PFC]

- Compare with 2-level, the 3-level topology has lower THD and reduced voltage stress
- Considering the unidirectional power flow and cost, the 3-level Vienna topology was selected

DC/DC Converter Topology

❑ Isolated DC/DC Converter Topology Comparison

	LLC Converter	Phase-shifted Full Bridge (PSFB)	Dual Active Bridge (DAB)	DAB in CLLC Mode
Device stress	High	Mild Low	Lowest	High
Transformer KVA rating	High	Medium	Low	High
capacitor RMS currents	High	Medium	Low	High
Bidirectional	No	No	Yes	Yes
Conduction losses	High	Medium	Lowest	Medium
Turn ON switching loss	ZVS	ZVS	ZVS	ZVS
Turn OFF switching loss	Low	High	High	Low
Control complexity	Moderate	Very simple	Simple to complex	Moderate
Wide Battery Voltage Fixed Bus Voltage	No	Yes	Yes	No
Paralleling Modules	Intensive	Easy	Easy	Intensive
Switching Frequency	High	High	High	High

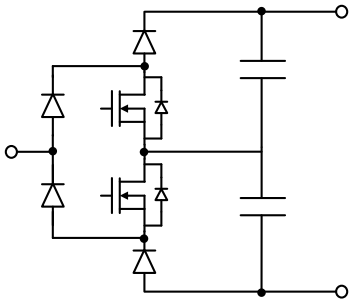
[Topology comparison of DC/DC converter]

- PSFB and DAB can achieve a wide output voltage range through simple phase-shift control
- The PSFB was selected because it is a unidirectional topology and suitable for paralleling multiple modules

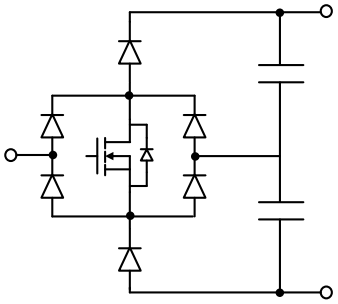
Contents

Hardware Design of AC/DC Vienna Rectifier

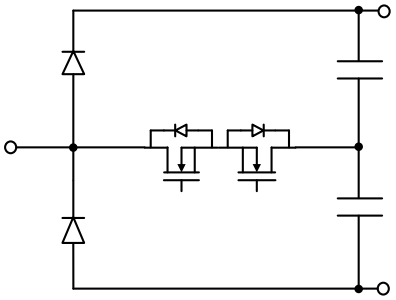
❑ Types of 3-Level Vienna (1-Phase)



[Type-A]



[Type-B]



[Type-C]

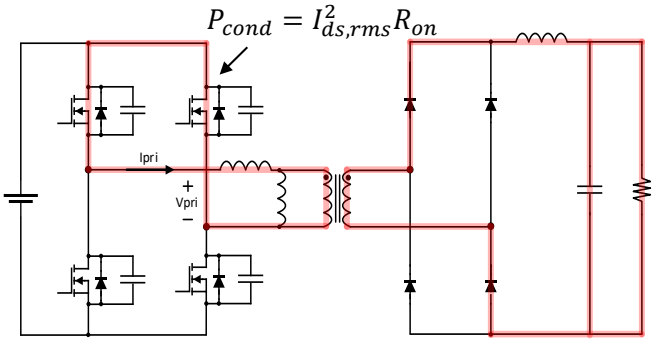
		Type-A	Type-B	Type-C
	# of diode	4	6	2
	# of MOSFET	2	1	2
for 800V dc-link	Diode maximum voltage	400	400	800
for 800V dc-link	MOSFET maximum voltage	400	400	400

- Type-C achieves the highest efficiency due to the lowest diode conduction loss
  - Efficiency : C > A > B
  - Cost : C > A > B

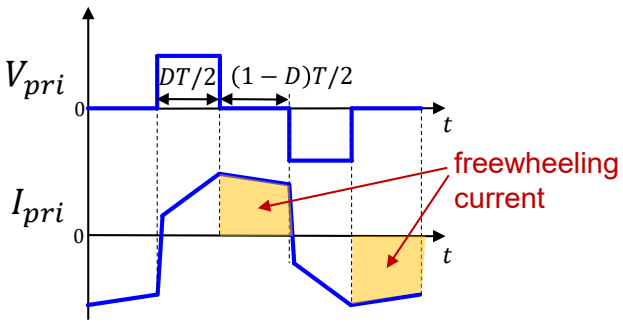
Hardware Design of DC/DC PSFB Converter

❑ Conduction Loss Issue Caused by Primary-Side Circulating Current

■ For low output voltage operation, a small duty ratio(D) is required, which increases conduction loss due to the large circulating current.



[Conventional PSFB freewheeling mode]



❑ Improvement Method

■ Current sharing using a primary-side parallel structure

- The total switch conduction loss is reduced to approximately half

[Conventional] [Parallel structure]

$$P_{cond} = 4 \times I_{ds,rms}^2 R_{on} \xrightarrow[\text{x1/2}]{} P_{cond} = 8 \times \left(\frac{I_{ds,rms}}{2}\right)^2 R_{on}$$

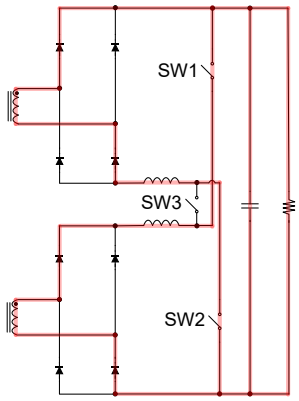
Hardware Design of DC/DC PSFB Converter

❑ High Voltage Stress Issue on Secondary-Side Diodes

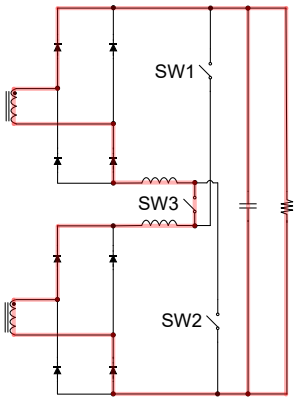
- High peak voltage occurs due to resonance between the transformer leakage inductance and the junction capacitance of the rectifier diodes
  - Peak voltage: $V_{DR,peak} = 2 \times \frac{N_s}{N_p} \times V_{dc}$
  - Ex.) $V_{dc} = 800[V]$, $\frac{N_s}{N_p} = \frac{10}{7}$ (for maximum 1000V output) → $V_{DR,peak} = 2286[V]$

❑ Improvement Method

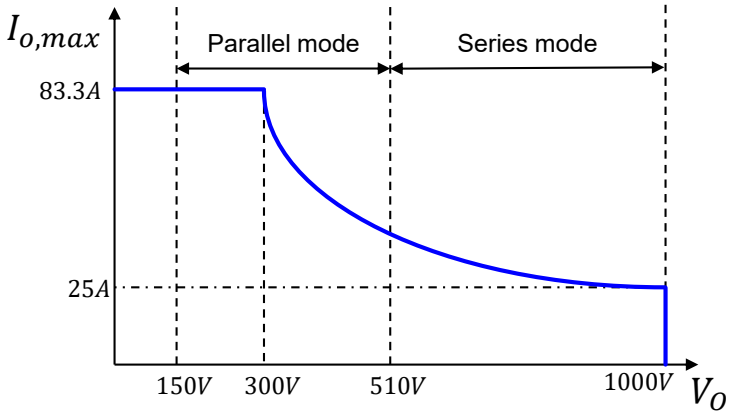
- Wide output voltage operation is achieved through secondary-side series/parallel mode change
- Redesign the transformer turns ratio : $\frac{N_s}{N_p} = \frac{5}{7}$ → $V_{DR,peak} = 1143[V]$, 1200V diodes can be used



[Parallel mode]



[Series mode]



[Operating mode according to output voltage]

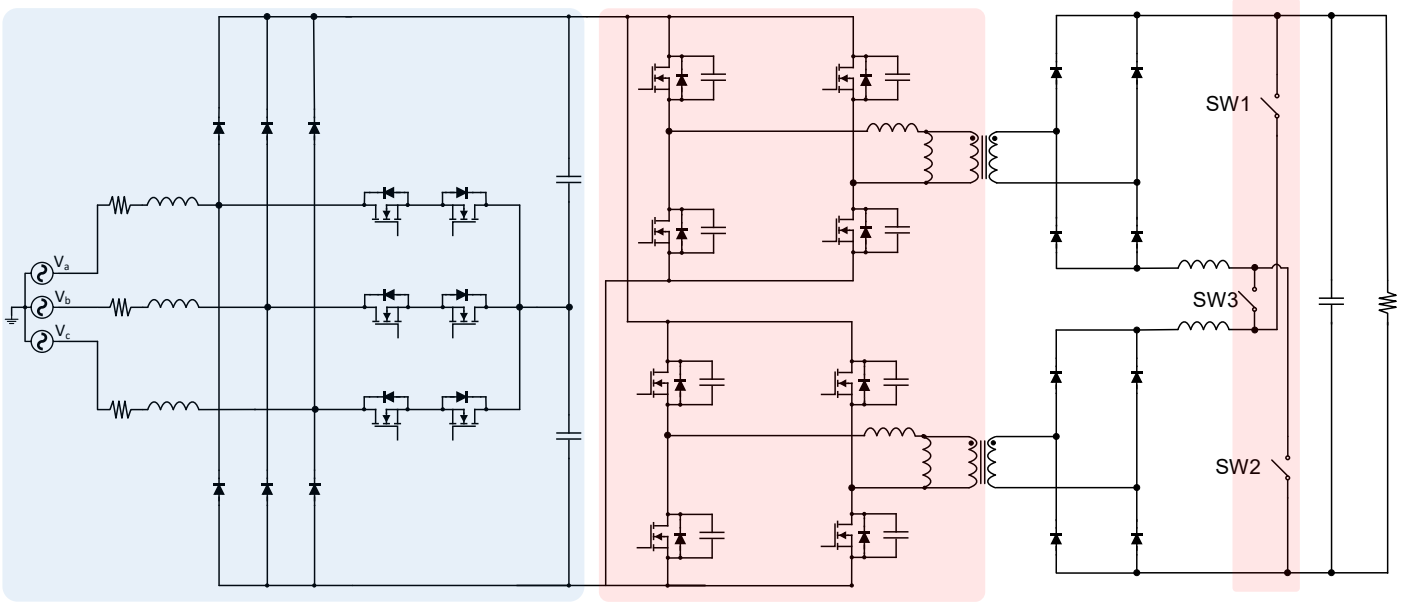
Hardware Design

❑ Proposed Circuit of 25kW Charging Module

3-pase 3-level Vienna rectifier

Primary-side parallel structure

Switches for secondary-side series/parallel mode change



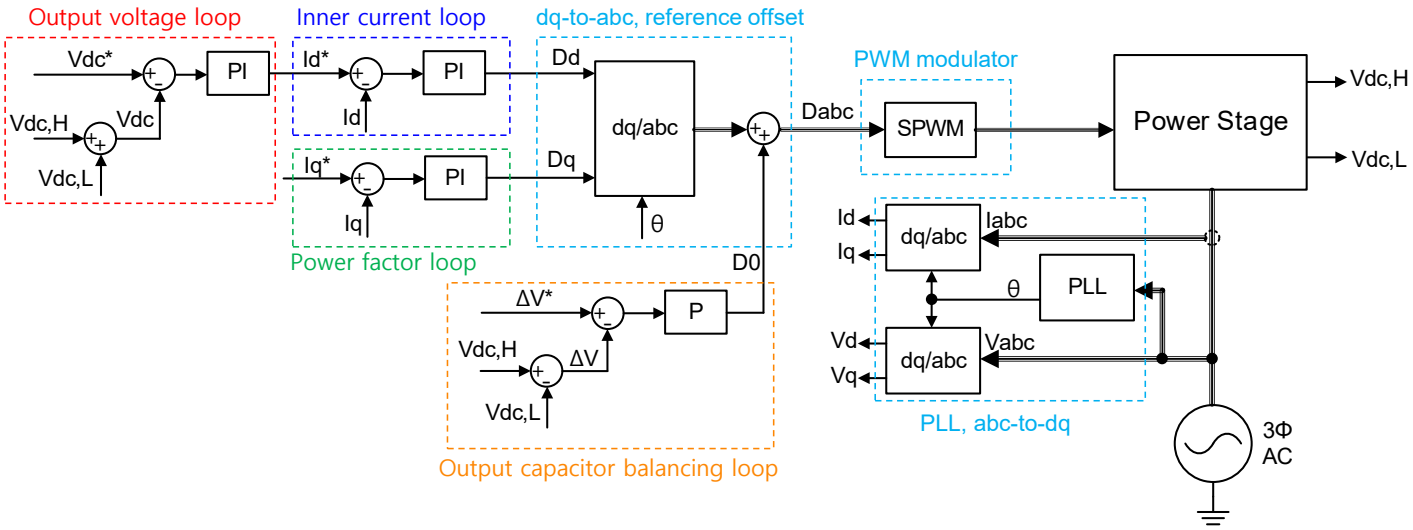
AC/DC side
3ph 3-level Vienna Rectifier

DC/DC side
Input parallel, output series/parallel PSFB

Control of AC/DC Vienna Rectifier

❑ 3-Phase Vienna Rectifier Control Structure

- DQ synchronous reference frame control
- Phase Locked Loop (PLL) : Detects the phase angle of the three-phase grid voltage
- Output voltage and input current control loops
- Power factor control loop (Iq*=0)
- Output capacitor voltage balancing loop (ΔV*=0)
- PWM modulator: Converts duty references into switch gate signals

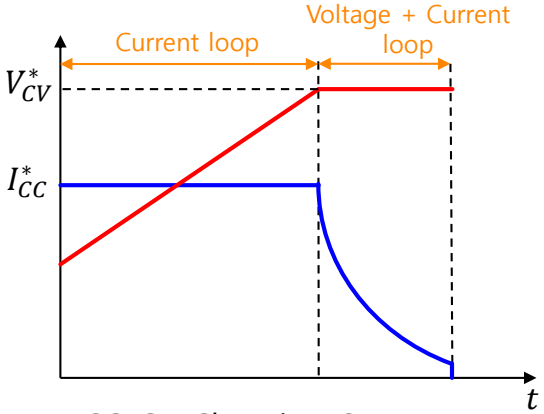


[Control Block Diagram of Three-Phase Vienna Rectifier]

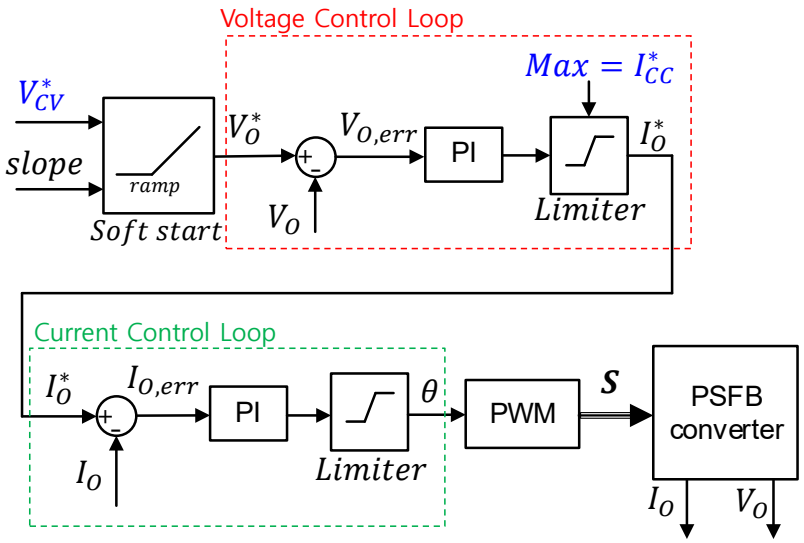
Control of DC/DC PSFB Converter

❑ PSFB Converter Control Structure

- Dual-loop PI control structure for output voltage and current control
- Voltage reference (V_{CV}^*) is set to the target battery voltage for CV charging
- Inrush current is minimized through soft-start during initial startup
- During CC charging, the voltage controller output is limited by the limiter → $I_o^* = I_{CC}^*$
- When the battery voltage (V_O) reaches the voltage reference (V_O^*), CV charging is performed
- The controller output is the phase-shift angle (θ)



[CC-CV Charging Sequence]

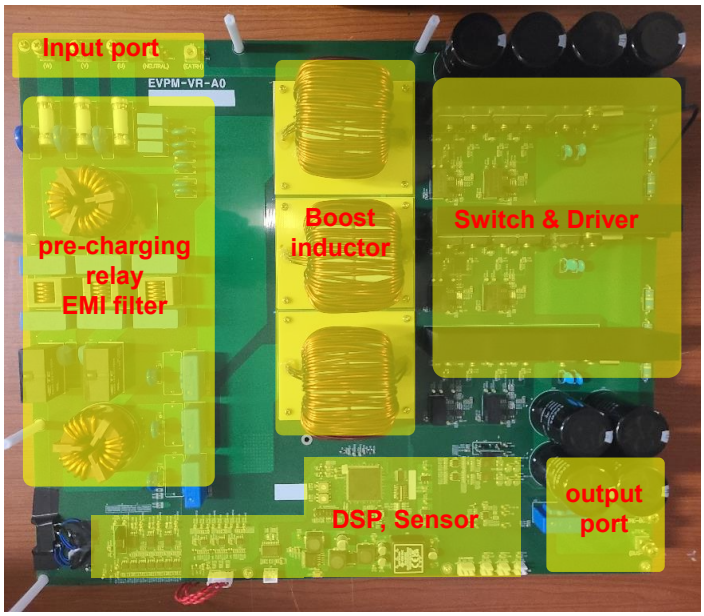


[Control Block Diagram of PSFB Converter]

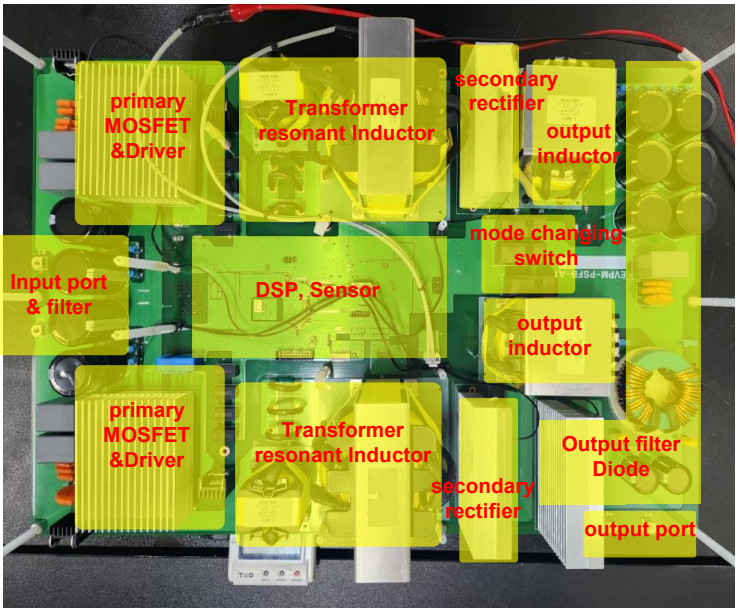
Contents

Prototype Hardware

❑ **Implemented Prototype Hardware**



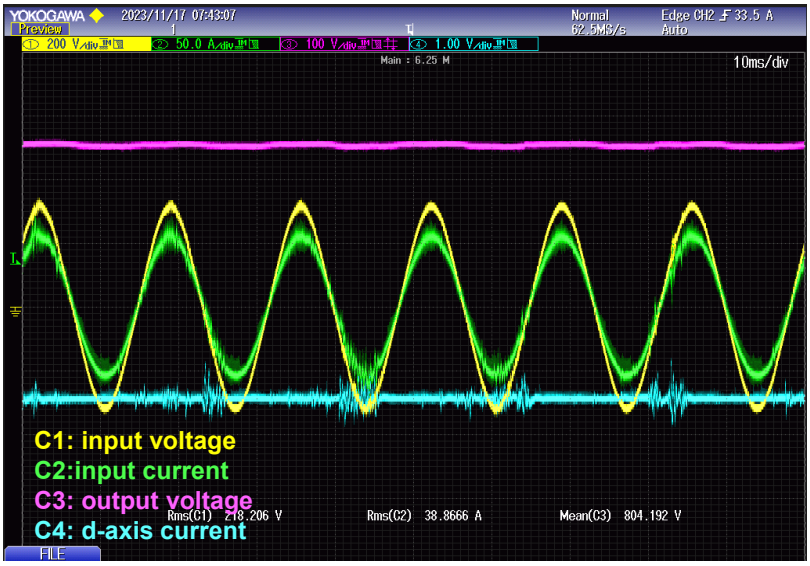
[25kW AC/DC Vienna Rectifier]



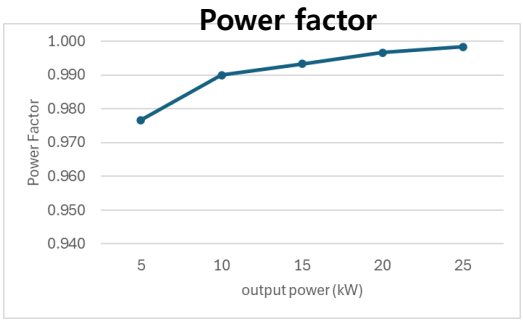
[25kW DC/DC PSFB Converter]

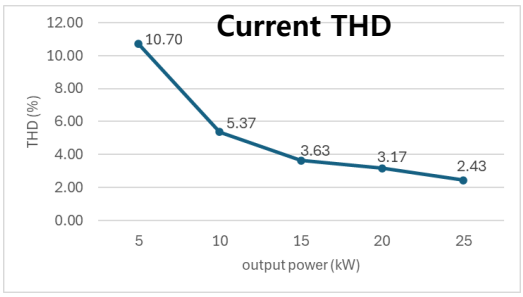
Experimental Results of AC/DC Vienna Rectifier

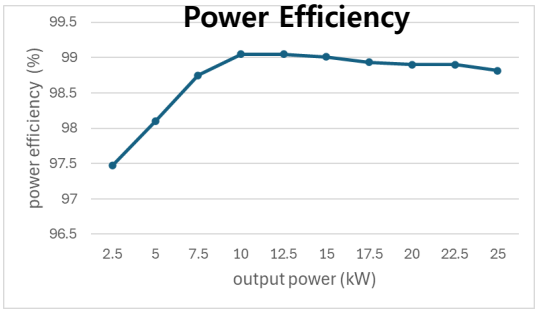
❑ Operation Test of 3-Phase Vienna Rectifier



[25kW operating waveforms]







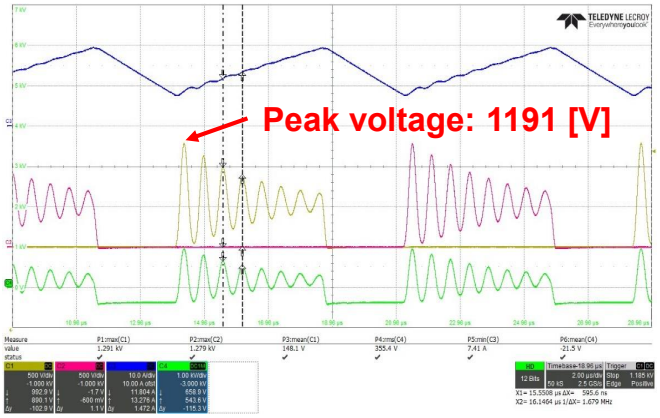
- Power factor: Over 0.99 at loads above 10 kW
- Current THD: 2.43% at 25 kW
- Efficiency: Maximum efficiency over 99%

Experimental Results of DC/DC PSFB Converter

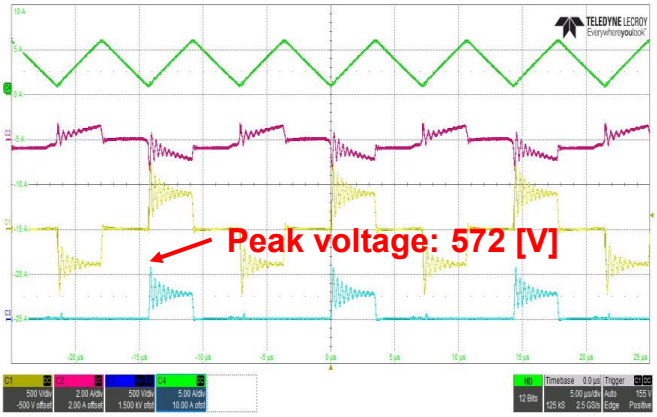
❑ Comparison of Secondary-Side Rectifier Diode Peak Voltage

■ Compared with a conventional PSFB converter under an input voltage of 400 V

[Conventional PSFB] $\frac{n_s}{n_p} = \frac{10}{7}$

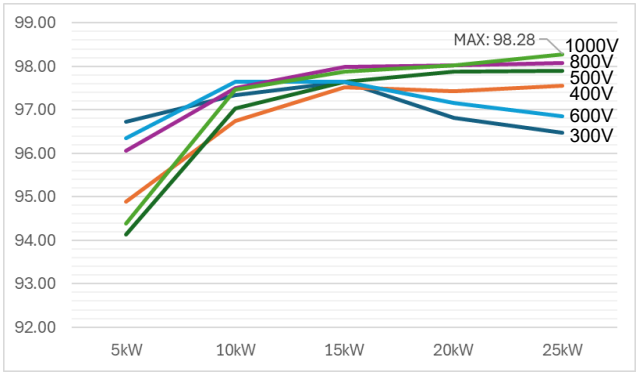


[Proposed PSFB] $\frac{n_s}{n_p} = \frac{5}{7}$

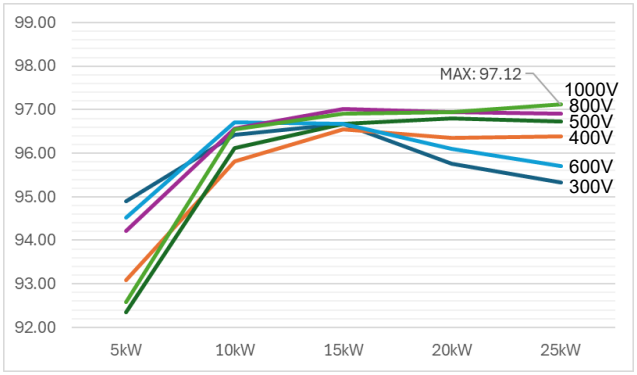


- The peak voltage is reduced by approximately 52% in the proposed PSFB converter

❑ Power Efficiency According to Output Voltage and Output Power



[DC/DC Converter Efficiency]



[Overall Efficiency of AC/DC + DC/DC Converter]

➢ A maximum overall efficiency of 97.12% was achieved at 1000 V and 25 kW output

Contents

Conclusion

❑ Proposed 25 kW Fast-Charging Module

- The primary side of the PSFB converter was designed with a parallel structure to reduce conduction loss caused by circulating current.
- The secondary side of the PSFB converter was designed with a series/parallel mode-change structure to achieve a wide output voltage range efficiently.
- The AC/DC converter achieved a maximum efficiency of over 99%, and the DC/DC converter achieved a maximum efficiency of 98.28%.
  - A maximum overall efficiency of 97.12% was achieved.

Thank you

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Design and Shape Optimization of Electromagnetic Bone Conduction Device Using Cantilever Structure

JUSW2026

May 19, 2026

Marin Ezaka*　　Wataru Kitagawa

(Nagoya Institute of Technology)

Outline

Mechanism of Bone Conduction

Bone Conduction Device

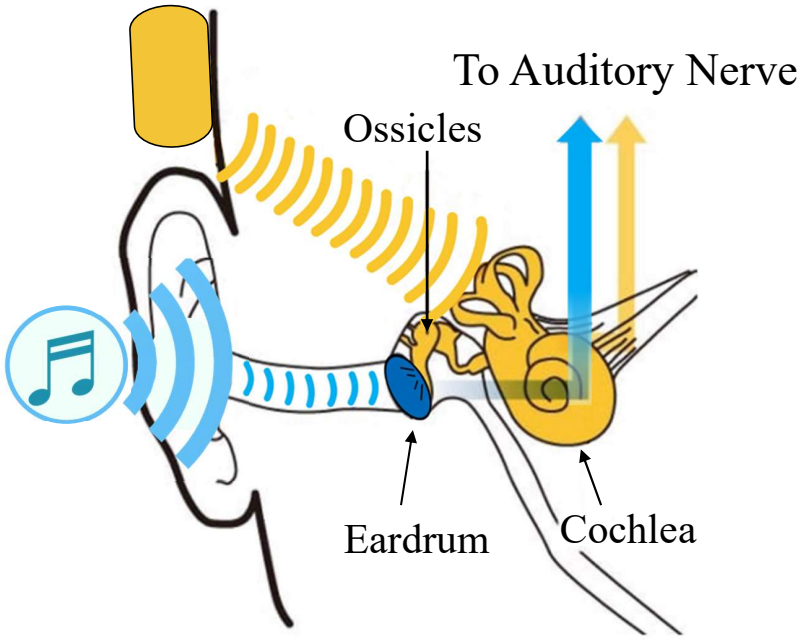
Bone vibration → Cochlea

→ Auditory nerve

Air Conduction

Air vibration→Eardrum→Cochlea

→Auditory nerve



Internal Structure of the Ear

Promising as a next-generation audio interface.

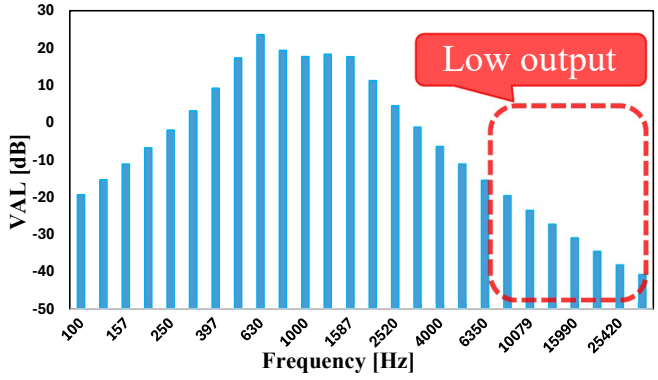
Research Background

Applications as Next-Generation Audio Interfaces

Audio Navigation Systems

Industrial Headsets

Ultrasonic Hearing Aids



Low output in high-frequency ranges.

➡ Shift to Cantilever structure

Realize a 2-way driving system.

➡ Adopt a dual-unit structure.

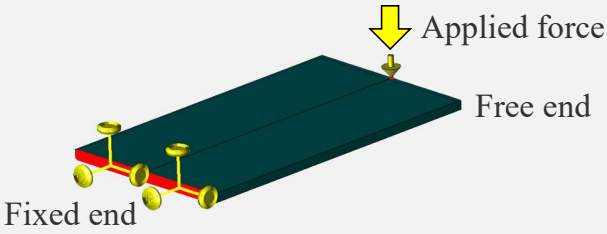
Goal: Improve output performance beyond the audible range(> 20 kHz).

Research Objectives

Features of Cantilever structure Device

① Diaphragm modification

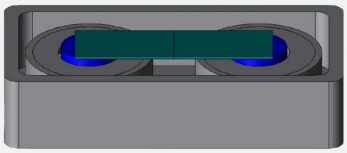
High output by using cantilever structure.



Improve high-frequency output by using a free-end design.

② Unit addition

High output by using dual-unit configuration.



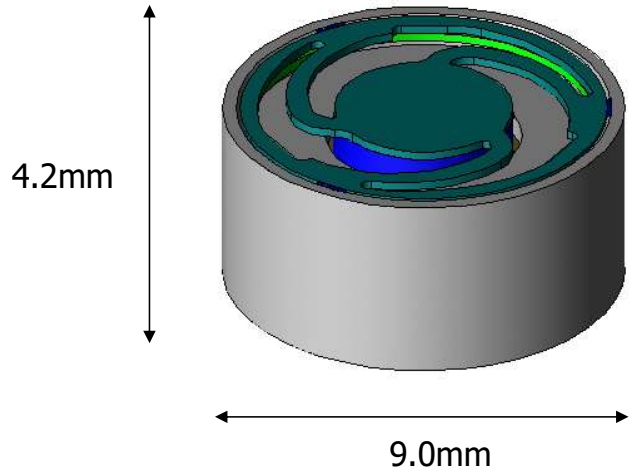
Adopt a dual-unit structure for future 2-way driving systems.

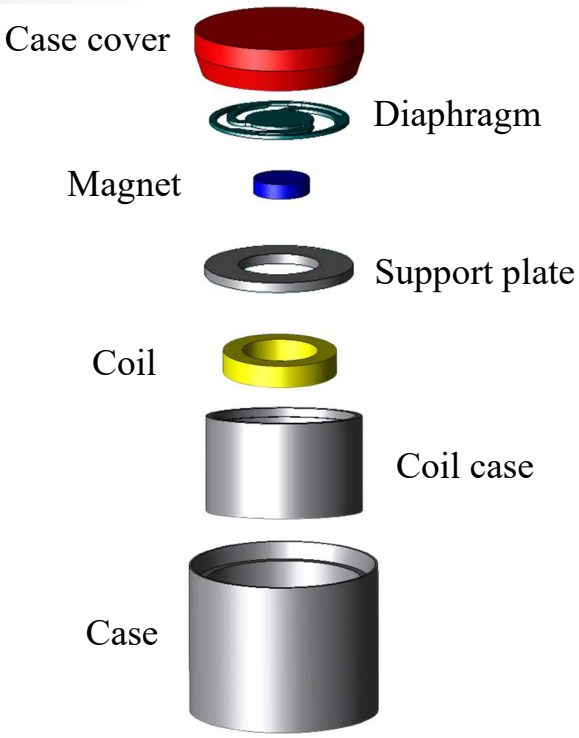
3D-FEM Analysis (Magnetic-Structural Coupling) ⟫ Experimental verification using a prototype.

Evaluate effectiveness through both theoretical and experimental approaches.

Outline

Circular Diaphragm Model



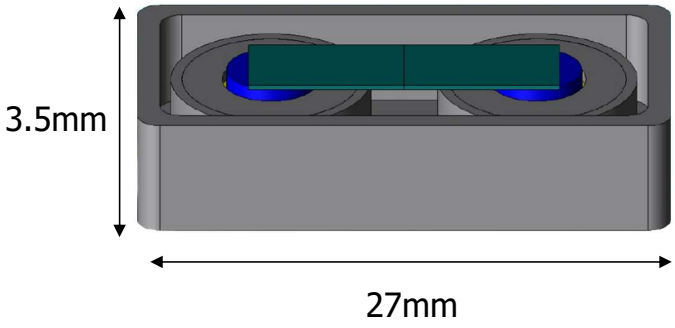


Challenge:

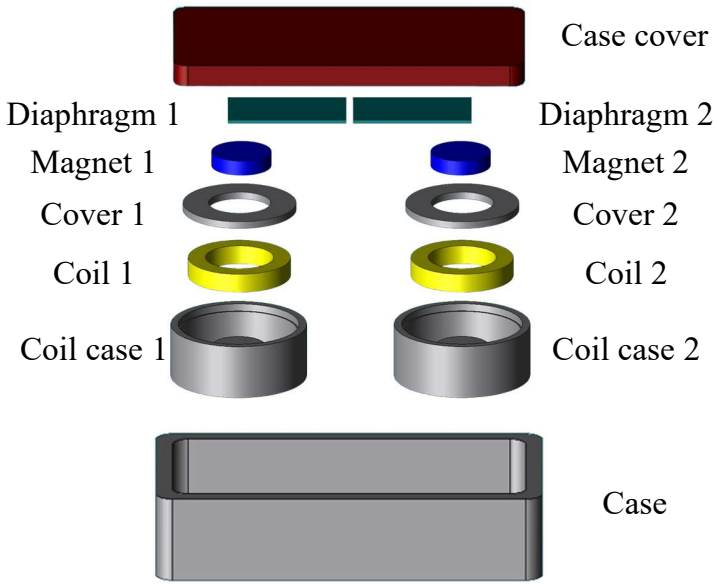
× Circular shape restricts the vibration amplitude.

× Short distance from the fix point reduces high-frequency output.

Cantilever Model



Overall View

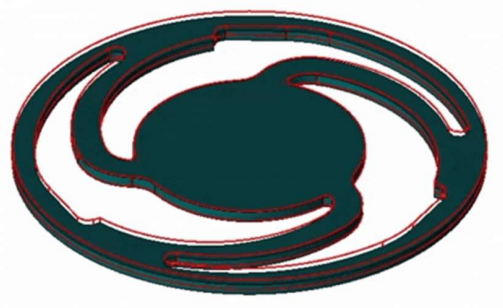


Exploded View

✓ Free-end design enables larger vibration displacement.

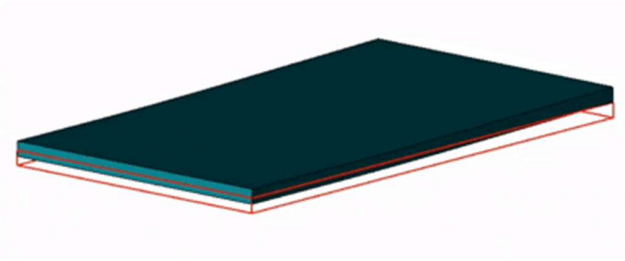
✓ Longer distance from the fix point maximizes output.

Comparison of Vibration Behavior



Circular Diaphragm
(Conventional Model)

Max Displacement:**0.032mm**

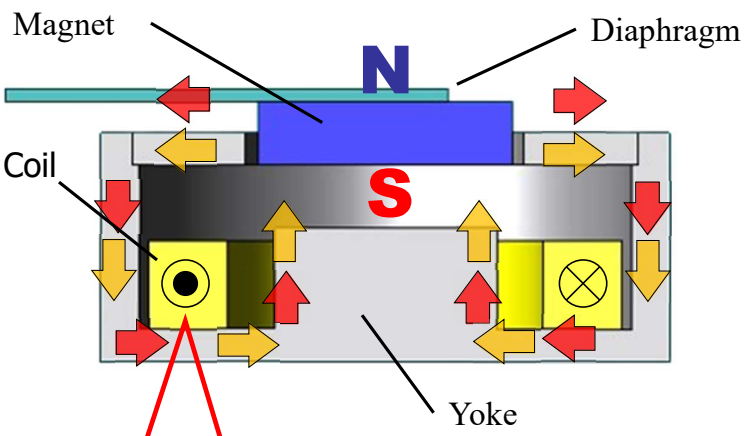


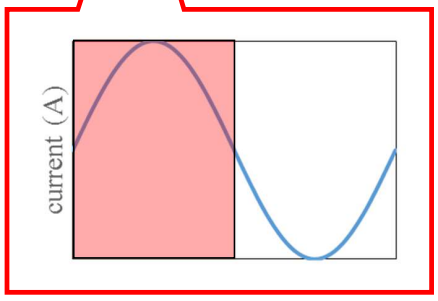
Cantilever (Proposed Model)

Max Displacement: **0.14mm**

- ✓ Larger amplitude due to longer distance from the support point.
- ✓ High displacement is achieved efficiently at high frequencies.

Operating Principle





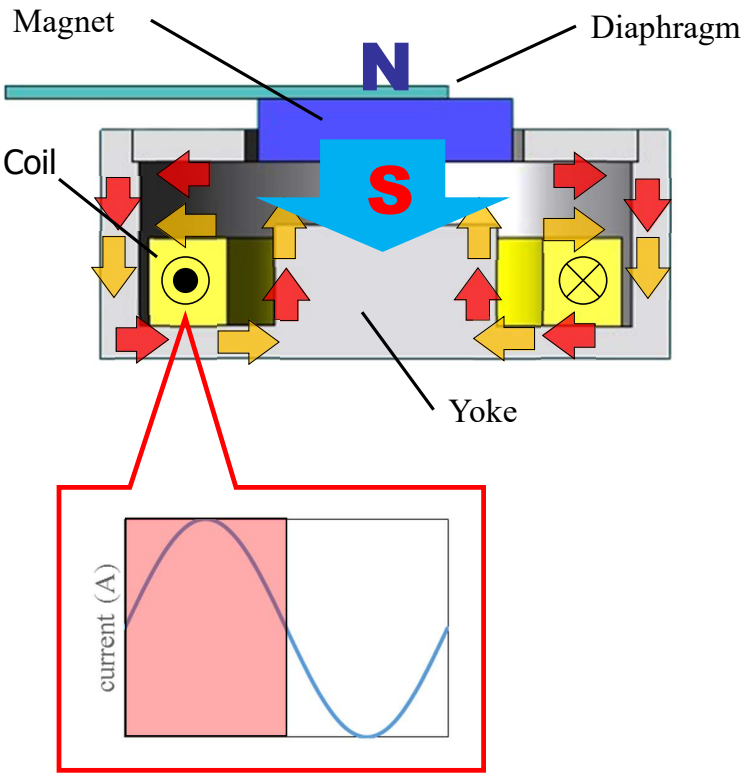
- Magnetic flux
- coil current flux
- Diaphragm displacement

Counter-clockwise current flows:

Magnetic fluxes in the yoke reinforce each other.

The diaphragm displaces downward.

Operating Principle



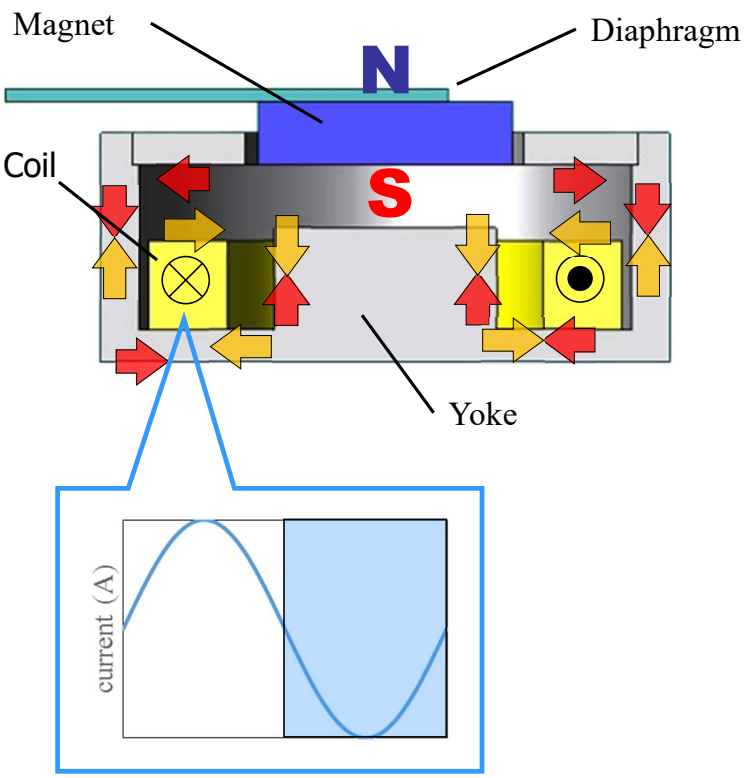
- Magnetic flux
- coil current flux
- Diaphragm displacement

Counter-clockwise current flows:

Magnetic fluxes in the yoke reinforce each other.

The diaphragm displaces downward.

Operating Principle



- Magnetic flux
- coil current flux
- Diaphragm displacement

Counter-clockwise current flows:

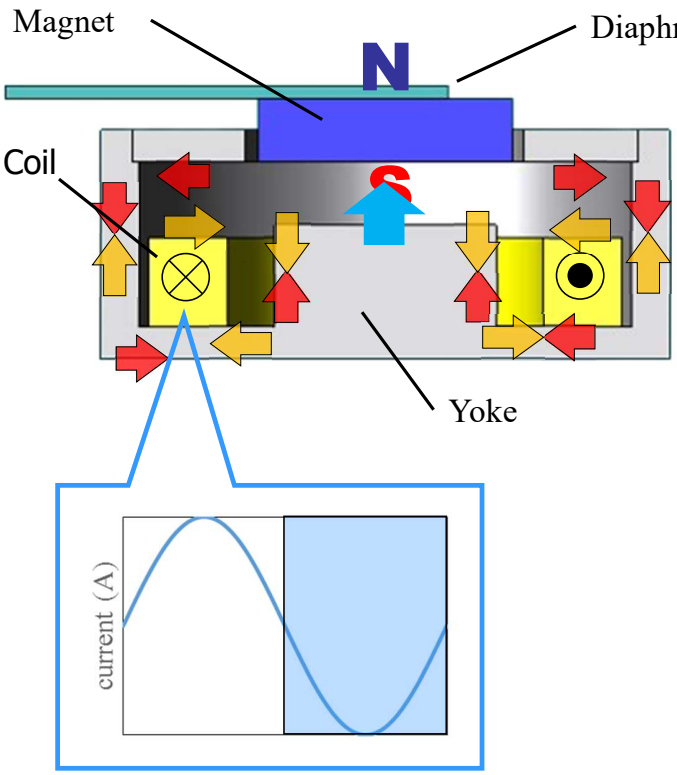
Magnetic fluxes in the yoke reinforce each other.

The diaphragm displaces downward.

clockwise current flows:

Magnetic fluxes in the yoke oppose each other.

Operating Principle



Magnetic flux

coil current flux

Diaphragm displacement

Counter-clockwise current flows:

Magnetic fluxes in the yoke reinforce each other.

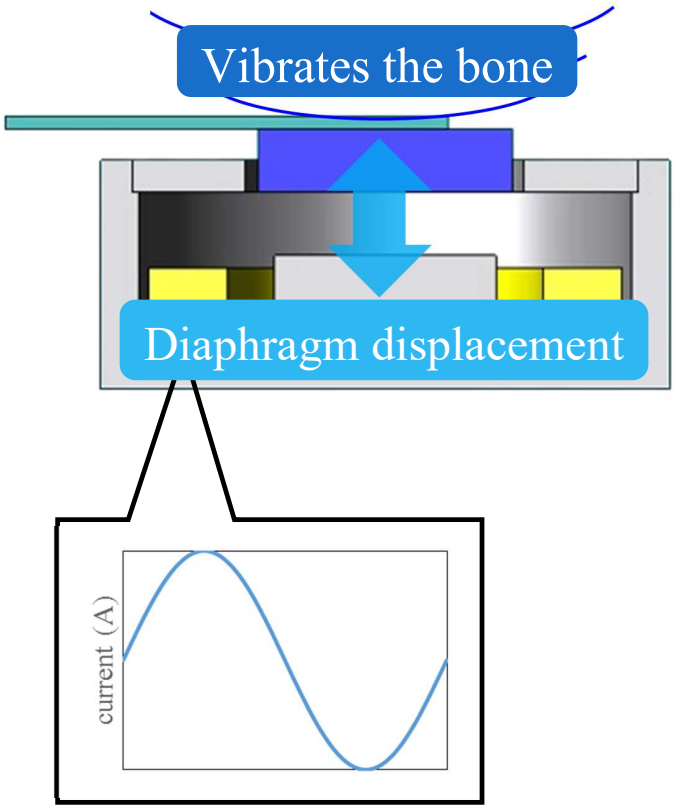
The diaphragm displaces downward.

clockwise current flows:

Magnetic fluxes in the yoke oppose each other.

The diaphragm displaces upward.

Operating Principle



Counter-clockwise current flows:

Magnetic fluxes in the yoke reinforce each other.

The diaphragm displaces downward.

Magnetic fluxes in the yoke oppose each other.

The diaphragm displaces upward.

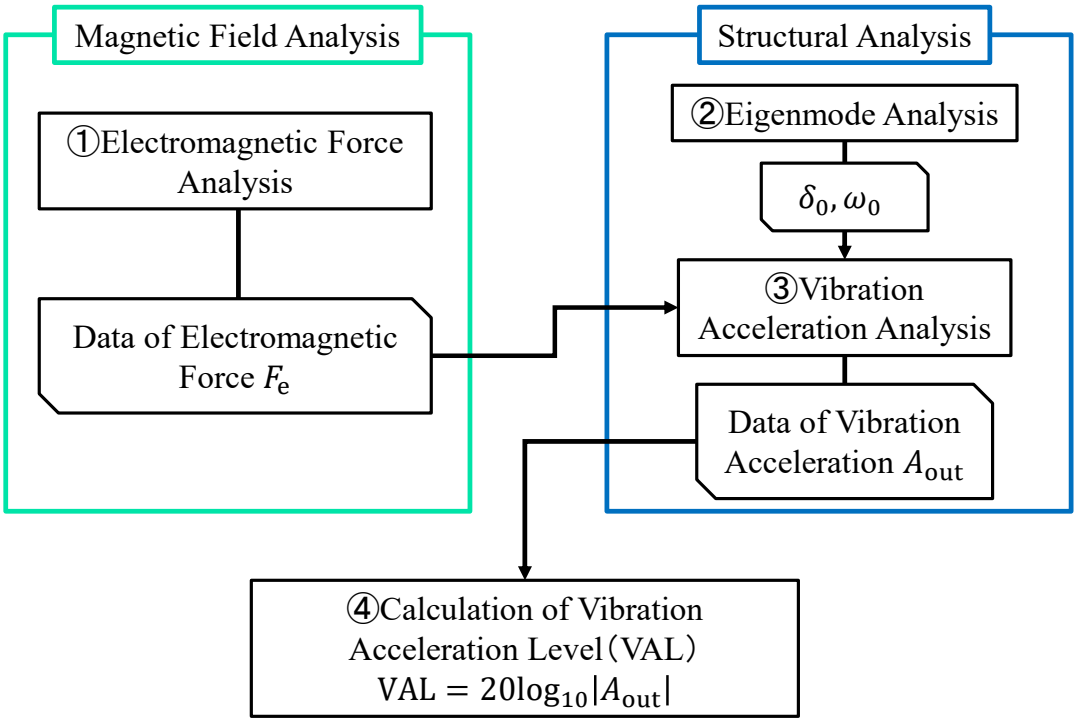
The attractive force between the yoke and magnet changes.

The diaphragm vibrates.

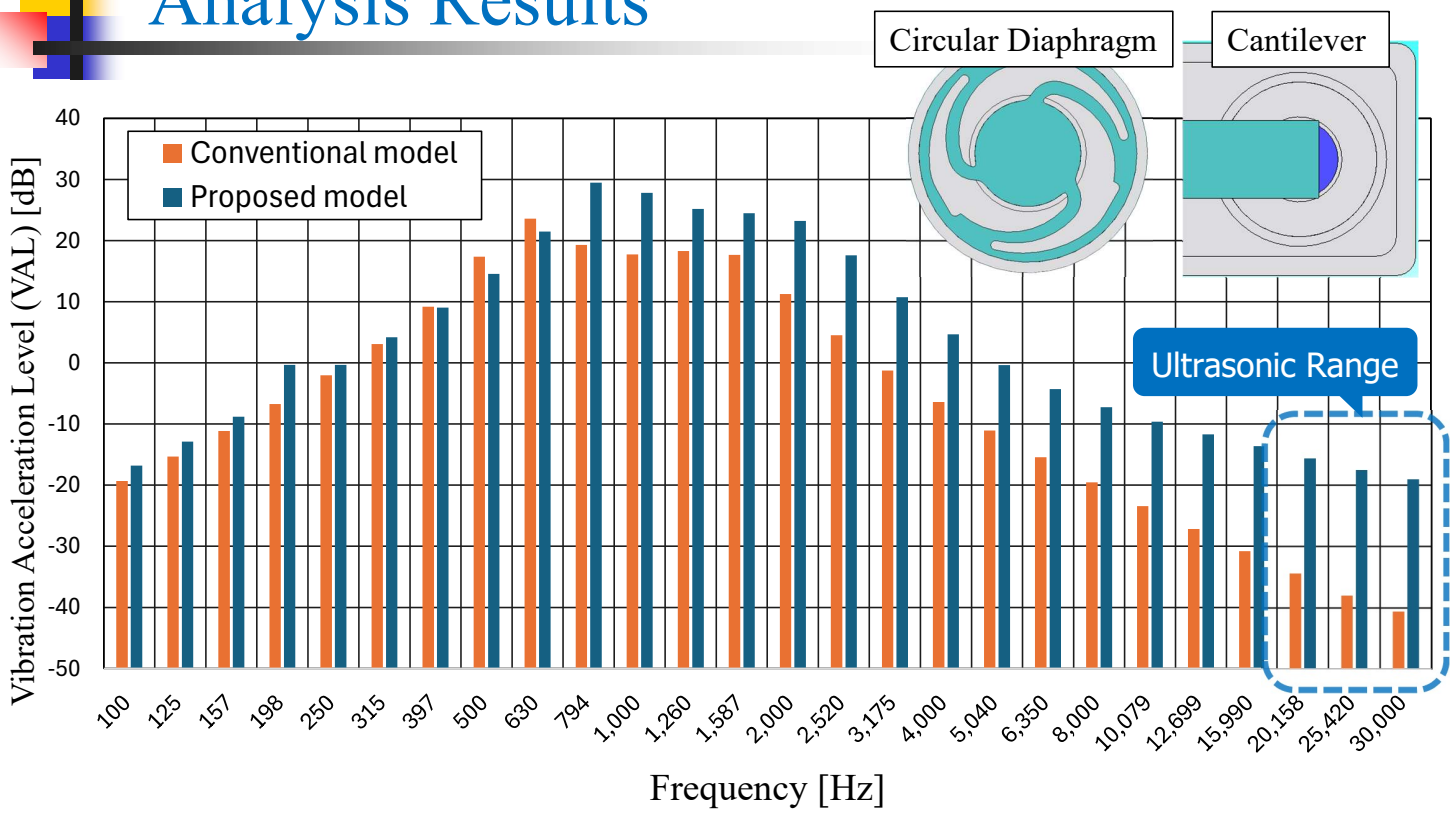
Sound is generated.

Outline

Analysis Method of Bone Conduction Devices

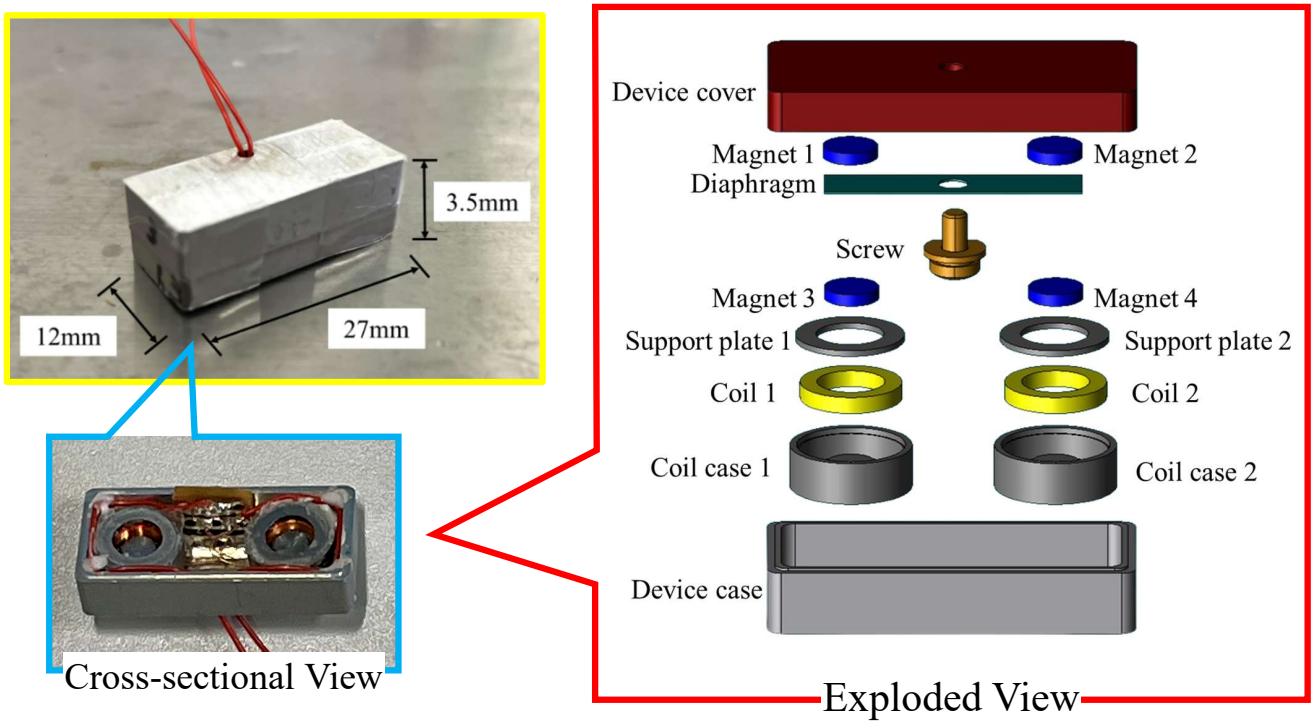


Analysis Results



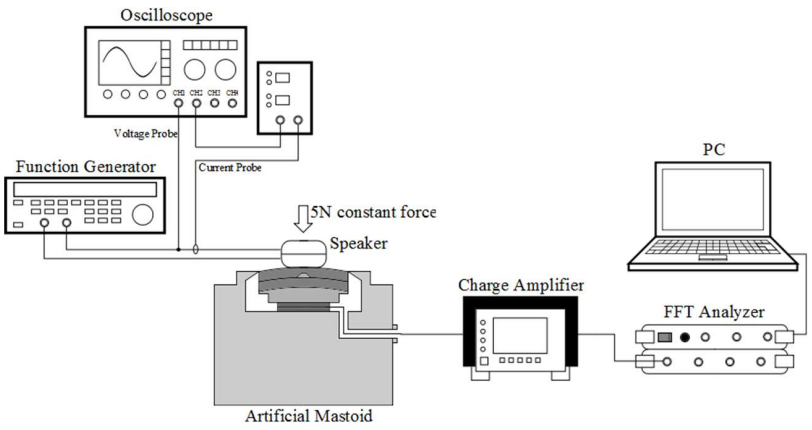
- ✓ Increased output in the high-frequency
- ✓ Resonance frequency: 794 Hz.

Cantilever Model: Prototype



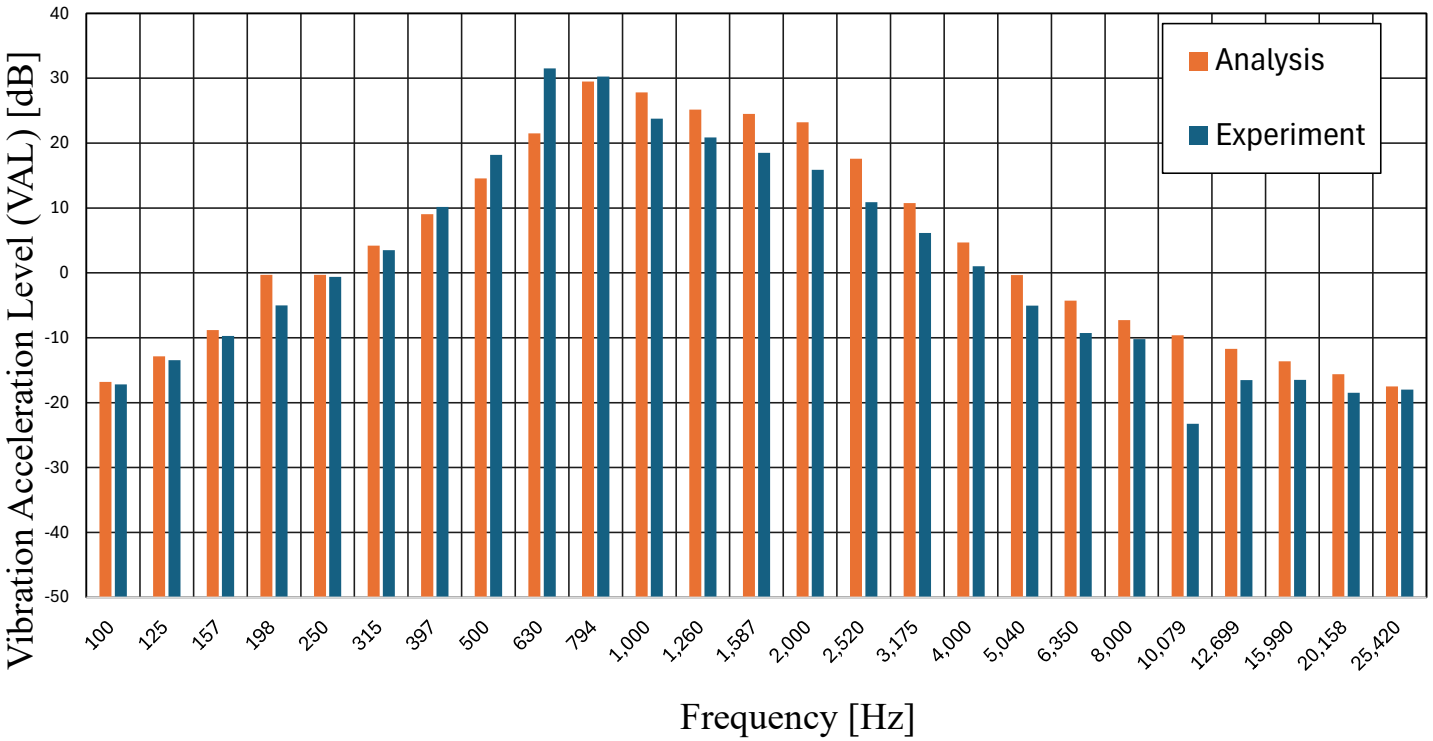
- ✓ The diaphragm is fixed with a screw.
- ✓ Two additional magnets were added to fix the diaphragm

Experimental Setup Overview



1. Measure output acceleration using an artificial mastoid.
2. Fix device to mastoid under 5 N constant load.
3. Apply sinusoidal voltage as a simulated audio signal.
4. Sweep 100–30,000 Hz in 1/3 octave steps.
5. Analyze frequency characteristics using an FFT analyzer.

Experiment vs. Analysis



✓ Generally matches analysis results

✓ Slightly lower resonance frequency

Outline

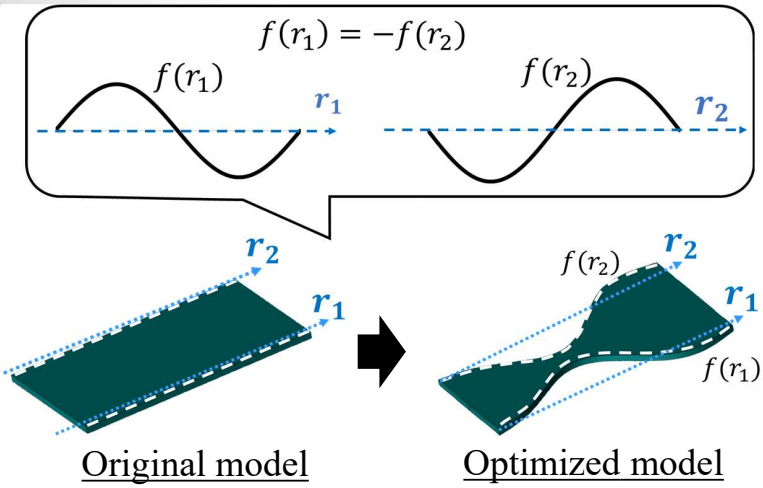
Mechanical Design Method using GA

➢Design Method

Diaphragm shapes $f(r_1)$ & $f(r_2)$ are defined by a trigonometric series:

$$f(x) = a_0 + \sum_{n=1}^{3} (a_n \cos p_n x + b_n \sin q_n x) \quad (0 \le x \le b_0)$$

(Amplitude: a_n, b_n; Frequency: p_n, q_n)



Original model → Optimized model

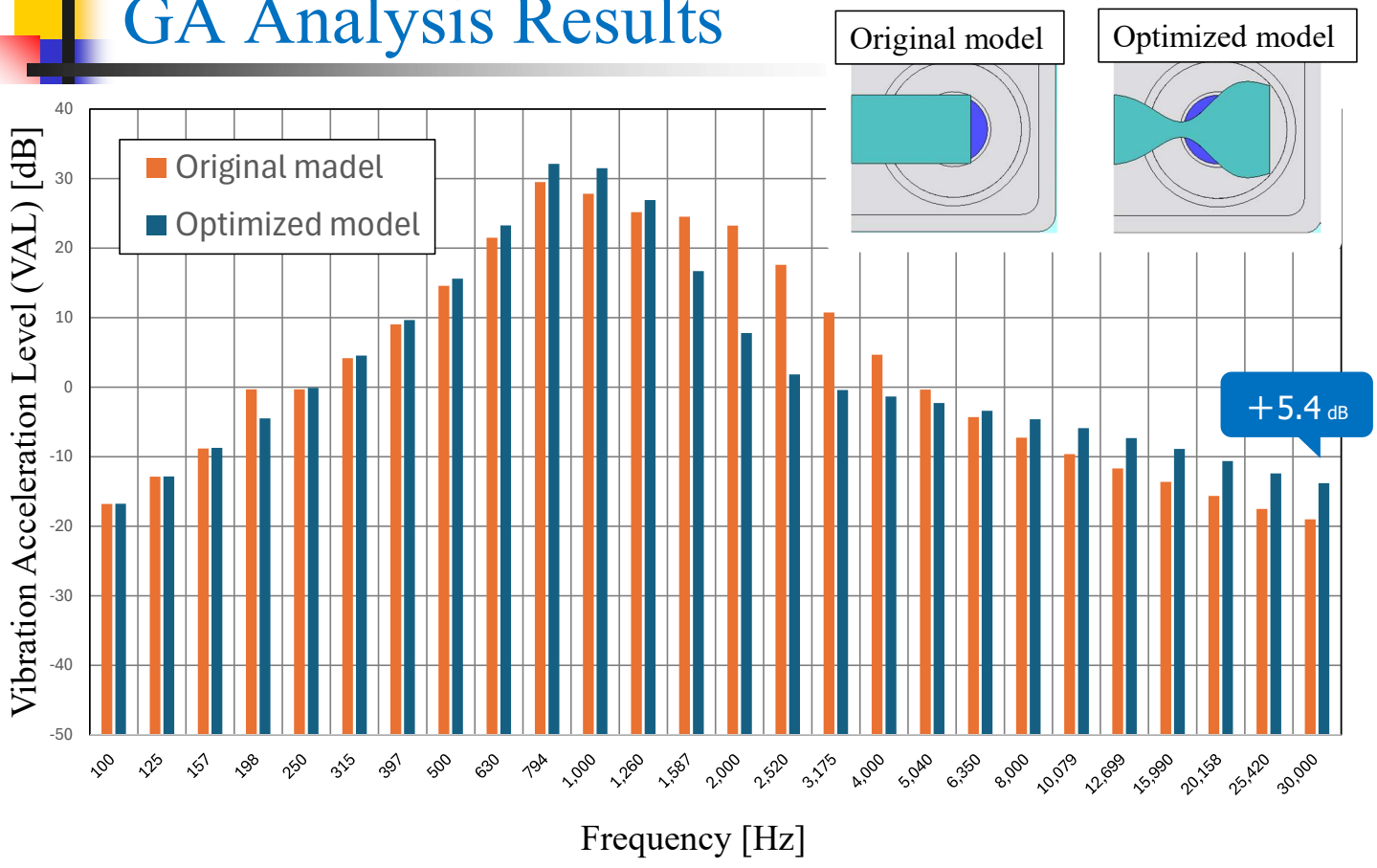
GA Conditions

- ✓ $f(r_1) = -f(r_2)$ (Symmetric shape)
- ✓ Objective function: Maximize VAL at 30kHz
- ✓ Parameters: Population :100
  Max generations :100
- ✓ Design variables: 14 variables (a_1~a_3, p_1~p_3, b_1~b_3, q_1~q_3)

Parameter	Value
a_0	0.5~2.5
a_1, a_2, a_3	−1~1
b_0	3~9
b_1, b_2, b_3	−1~1
p_1, p_2, p_3	−3~3
q_1, q_2, q_3	−3~3

Shape optimization using 14 variables to improve output.

GA Analysis Results



✓ VAL increased by 5.4 dB at 30 kHz.
✓ Decreased in the range of 1587–5040 Hz.

Conclusion

Objectives & Results

Optimization of the proposed model and measurement of the prototype to improve high-frequency output of bone conduction devices.

- Improved high-frequency output over the conventional model.
- Confirmed effectiveness through prototype measurement.
- Shape optimization improved VAL by 5.4 dB at 30 kHz.

Future Work

- GA optimization using multiple objective functions.
- Optimal design and prototype fabrication for 2-way drive.

Joint University Student Exchange Program

Design of a Quantile Regression Forecasting-based Robust EMS for Large-Scale Loads

Seongggyeol Kim · Yubin Lee

Future Power Network And Economics Lab. Chungbuk National University

충북대학교 CHUNGBUK NATIONAL UNIVERSITY

Contents

1. Background

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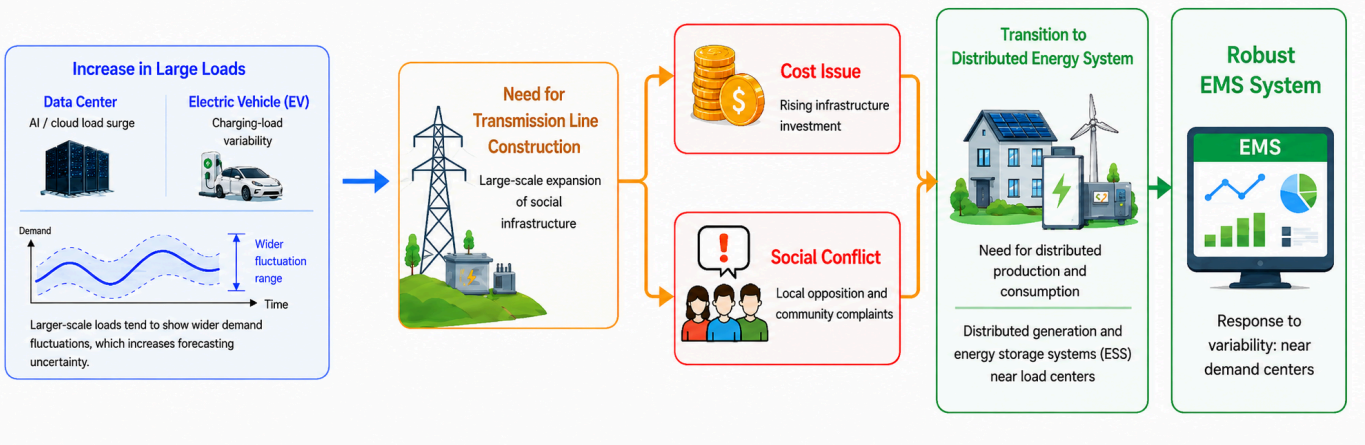
01. Background

■ Background

- Rapid growth of large-scale loads, such as data centers and EV charging infrastructure
- Concern over increased load variability risk due to large-scale load growth
- Need for distributed energy production and consumption near major load centers
- Necessity of a robust EMS for reliable operation under load variability

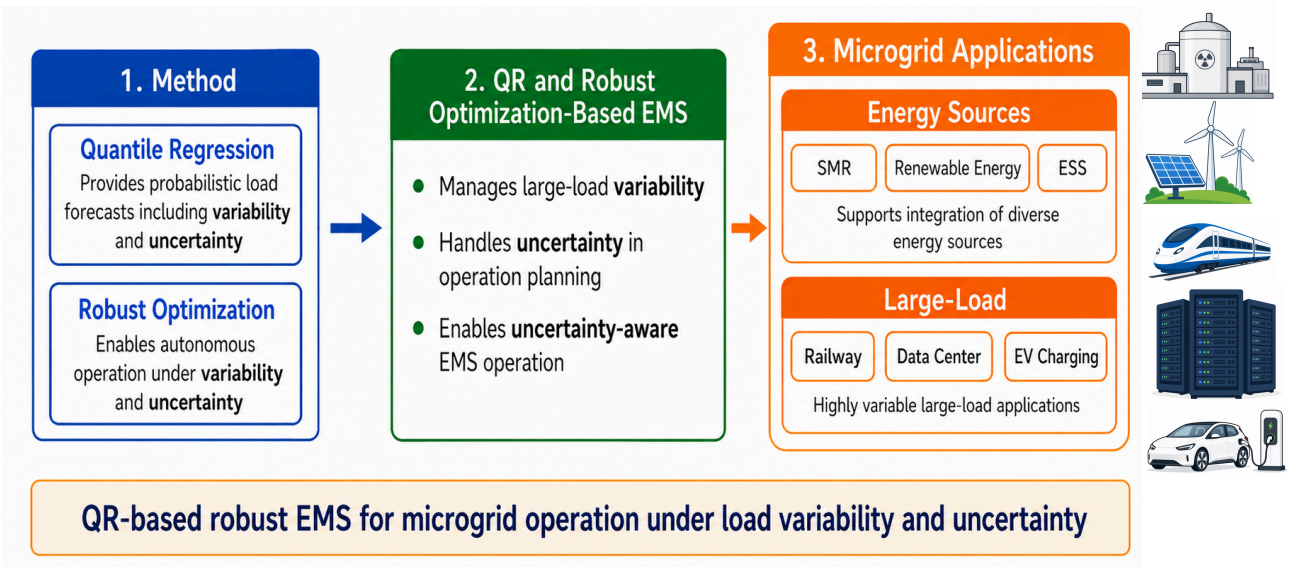


4

01. Background

■ Research's Goal

- Design of a QR(Quantile Regression) based robust EMS for managing variability and uncertainty of large-scale loads



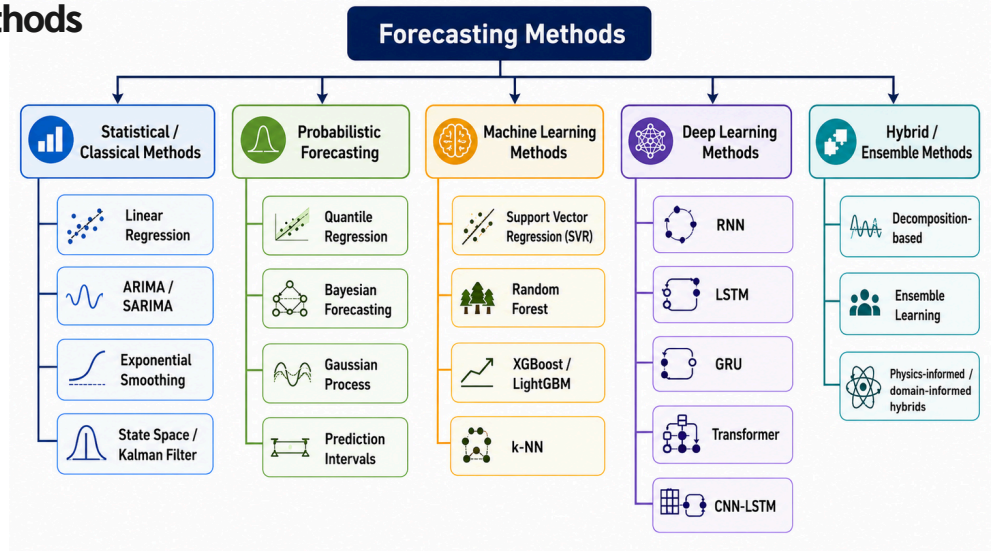
2. Quantile Regression

02. Quantile Regression

■ Importance of Forecasting Methods

- Growing importance of load forecasting with increasing load variability
- Provision of key input data for EMS operation and optimization under uncertainty

■ Various Forecasting Methods

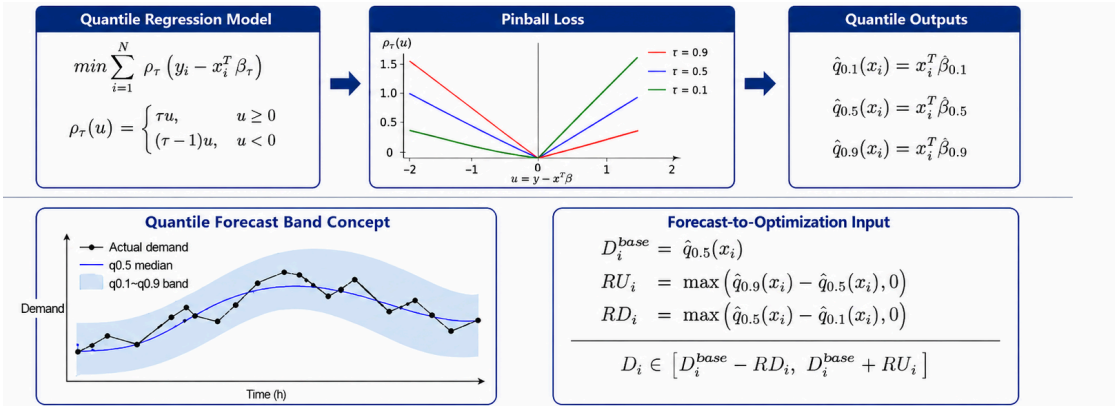


02. Quantile Regression

■ Quantile Regression

- Point forcasting : Single expected value → Limited uncertainty representation
- Quantile Regression : Conditional quantile estimation → Genration of prediction band

→ **Selection rationale** : Explicit representation of variability and forecasting uncertainty



Derivation of reserve requirements from quantile prediction bands

※ reserve : Standby capacity margin defined by the spread between median and boundary quantiles

■ Forecast Evaluation

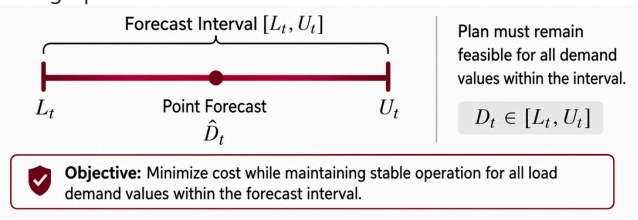
Metric	Formula	Interpretation
PICP	$PICP = \frac{1}{N}\sum_{i=1}^{N} \varepsilon_i \quad \varepsilon_i = \begin{cases} 1, & if\ y_i \in [L_i, U_i]; \\ 0, & if\ y_i \notin [L_i, U_i]. \end{cases}$	**Meaning** : Coverage probability **Desirable property** : Close to the nominal confidence level
PINAW	$\mathrm{PINAW} = \frac{1}{m(\max(y_{ij}) - \min(y_{ij}))}\sum_{i=1}^{m}(\mathrm{UL}_{ij} - \mathrm{LL}_{ij}), j = 1, \ldots, k.$	**Meaning** : Normalized width of the prediction interval **Desirable property** : Minimum value
PINAD	$\mathrm{PINAD} = \frac{1}{m}\sum_{i=1}^{m}\frac{D_{ij}}{\max(y_{ij}) - \min(y_{ij}}$ $D_{ij} = \begin{cases} \mathrm{LL}_{ij} - y_{ji}, & \text{if } y_{ji} < \mathrm{LL}_{ij}, \\ 0, & \text{if } \mathrm{LL}_{ij} \le y_{ji} \le \mathrm{UL}_{ij}, \\ y_{ji} - UL_{ij}, & \text{if } y_{ji} > \mathrm{UL}_{ij}. \end{cases}$	**Meaning** : Magnitude of deviation outside the prediction interval **Desirable property** : Minimum value, ideally close to zero
Winkler Score	$WS = \begin{cases} D_t, & L_t \le y_t \le U_t \\ D_t + \frac{2(L_t - y_t)}{\alpha}, & y_t < L_t \\ D_t + \frac{2(y_t - U_t)}{\alpha}, & y_t > U_t \end{cases}$	**Meaning** : Overall score for interval forecast quality **Desirable property** : Minimum value

3. Robust Optimization

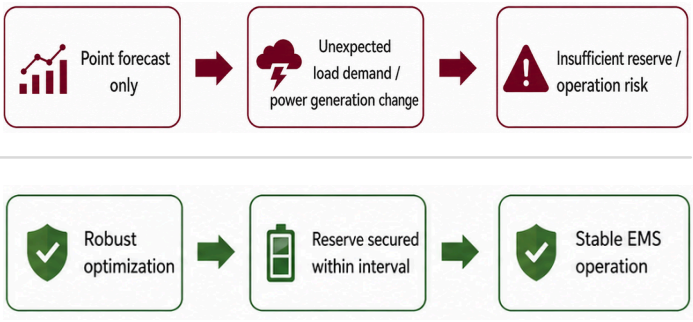
03. Robust Optimization

■ What is Robust Optimization

- Derivation of feasible operational solutions via uncertainty sets under demand and power generation uncertainty
- Consideration of quantile–based prediction bands instead of reliance on a single point forecast



■ Why is it needed?



1 Railway Station

Train schedules, HVAC, passenger flow, and station facilities cause rapid load fluctuations.

Robust optimization helps ensure reserve against unexpected peak demand.

2 Data Center

Computing demand and cooling load can rise simultaneously, increasing power uncertainty.

Robust optimization improves reliable operation under sudden demand surges.

3 EV Charging Hub

Vehicle arrival time, charging duration, and charging power are difficult to predict.

Robust optimization prepares the EMS for high-demand charging scenarios.

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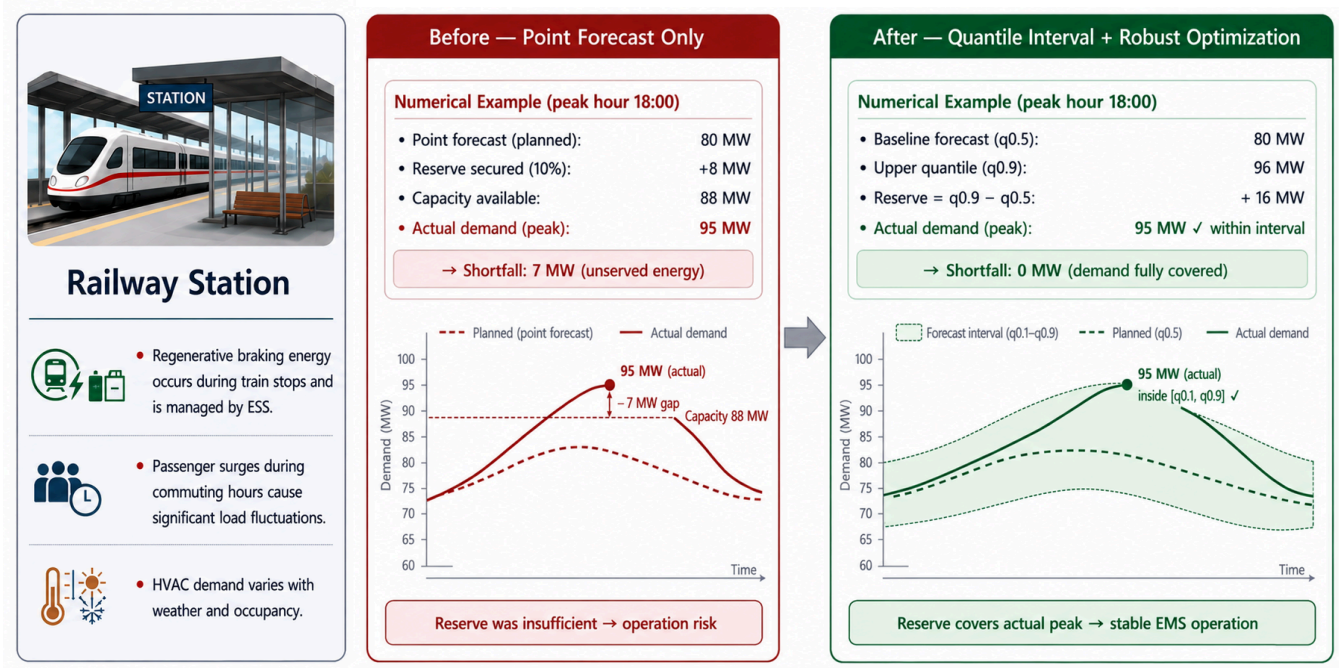
03. Robust Optimization

■ Advantages of Applying Robust Optimization – Case Study: Railway Station



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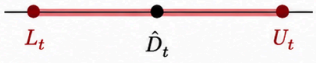
■ Robust Optimization

1. Forecast Interval and Reserve Requirement



$$L_t = q_{low,t}, \quad \hat{D}_t = q_{0.5,t}, \quad U_t = q_{high,t}$$

$$D_t \in [L_t, U_t]$$

$$RU_t = \max(U_t - \hat{D}_t, 0)$$

$$RD_t = \max(\hat{D}_t - L_t, 0)$$

- Quantile forecasts represent demand uncertainty as an interval.
- The interval is converted into upward and downward reserve requirements.

2. Robust Optimization Formulation

Objective

$$\min \sum_t \left[C_{gen}(P_t) + C_{ESS}(ch_t, dis_t) + C_{pen} \cdot x_t \right]$$

Main constraints

$$P_t + dis_t - ch_t = \hat{D}_t$$

$$RU_t^{plan} \geq U_t - \hat{D}_t$$

$$RD_t^{plan} \geq \hat{D}_t - L_t$$

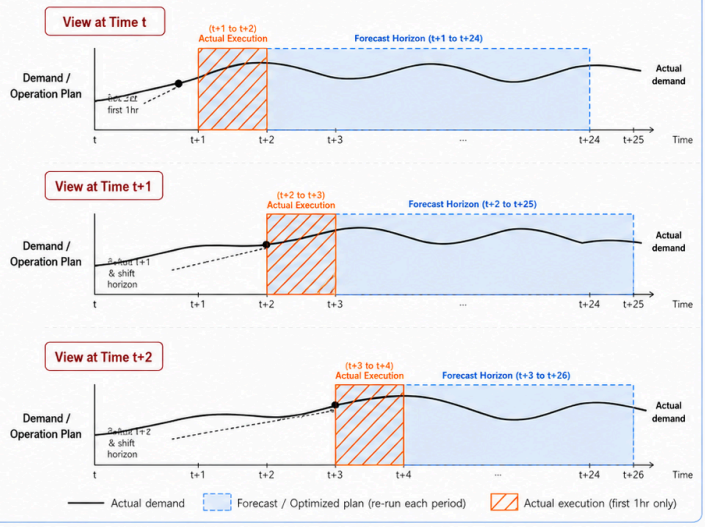
$$SOC_{t+1} = SOC_t + \eta_{ch} ch_t - dis_t / \eta_{dis}$$

$$P_t^{min} \leq P_t \leq P_t^{max}$$

$$SOC^{min} \leq SOC_t \leq SOC^{max}$$

3. Rolling-Horizon Optimization

- Re-forecast and re-optimize every hour
- Execution of only the first-hour decision
- Shift the horizon forward and repeat



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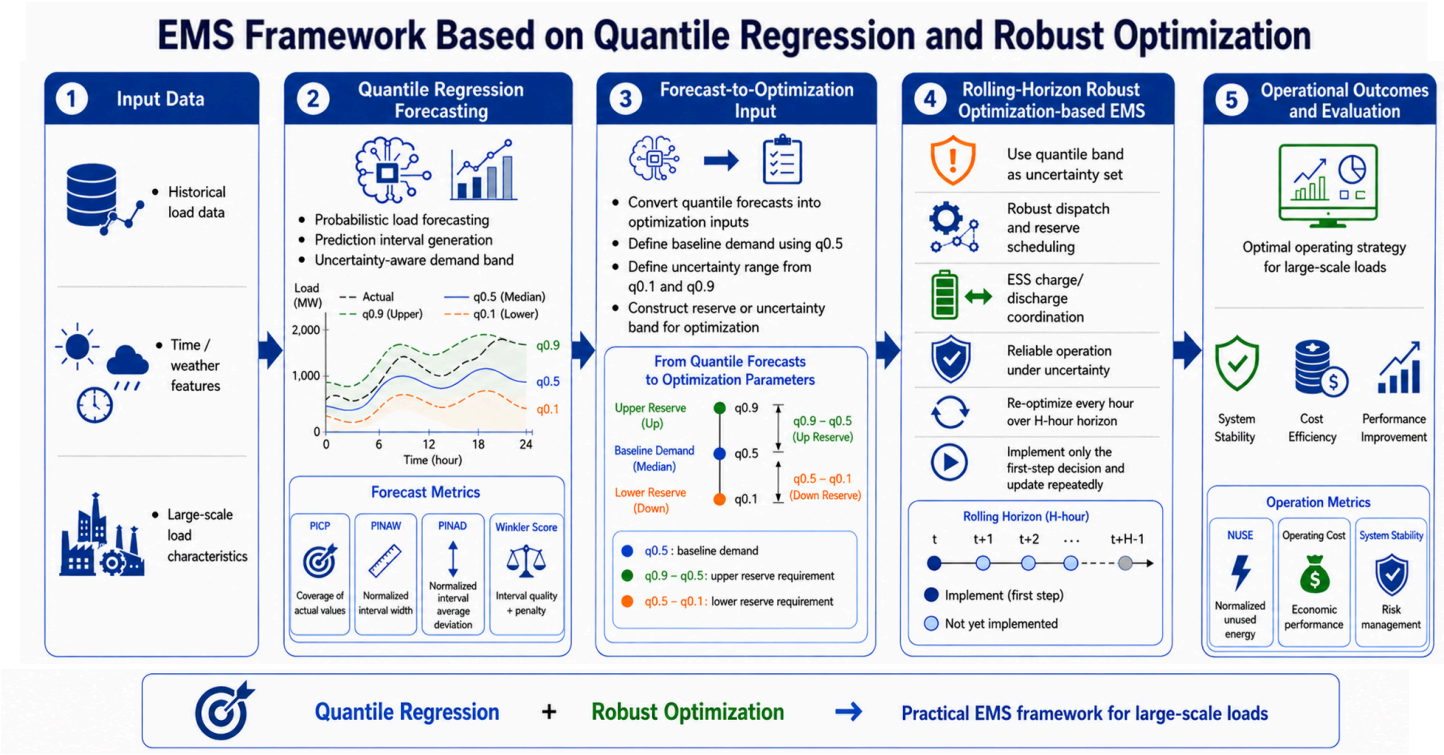
4. EMS Framework Implementation

14

04. EMS Framework Implementation



15

5. Simulation

16

05. Simulation

■ DATA

1. Data Source

- Korea Power Exchange (KPX) public data
- Nationwide hourly power demand data
- Data fields: date, time, power demand (MWh)
- 2020 and 2021 data were downloaded separately and then merged

2. Overview of the Dataset

Dataset	KPX nationwide power demand
Time period	Jan. 1, 2020 – Dec. 31, 2021
Training data	2020 (1 year)
Test / validation	2021 (1 year)
Resolution	1 hour
Total data points	17,543
Unit	MWh
Target variable	System load (Demand)
Forecasting features	lag1, lag24, lag168, hour, sin, hour_cos

3. Data Scaling

Purpose	Adapt nationwide demand data to a microgrid-scale EMS environment
Original peak demand	94,500 MW
Target peak demand	101 MW
Method	Temporal pattern preserved, only magnitude reduced
Main use	Quantile forecasting for interval-based robust EMS optimization

Scaled demand = Original demand × (101 MW / Original peak demand)

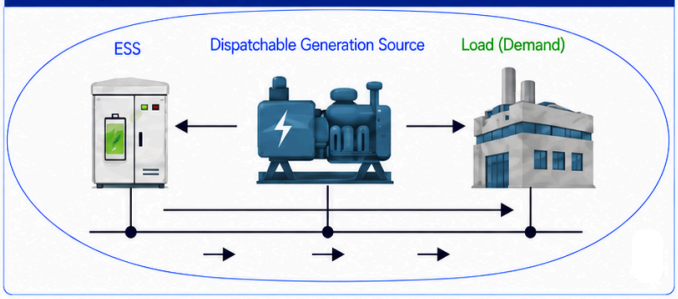
Scaled demand = Original demand × (101 MW / 94,500 MW)

4. Simulation Resource Parameters

Dispatchable Generation Source	
Maximum output	100 MW
Minimum output	10 MW
Ramp rate	10 MW/h
Generation cost	75,000 KRW/MWh

ESS	
Energy capacity	24 MWh
Max charge / discharge power	24 MW
Charge efficiency	0.97
Discharge efficiency	0.97
SOC range	10% ~ 90%
Initial SOC	50%

5. Microgrid Configuration



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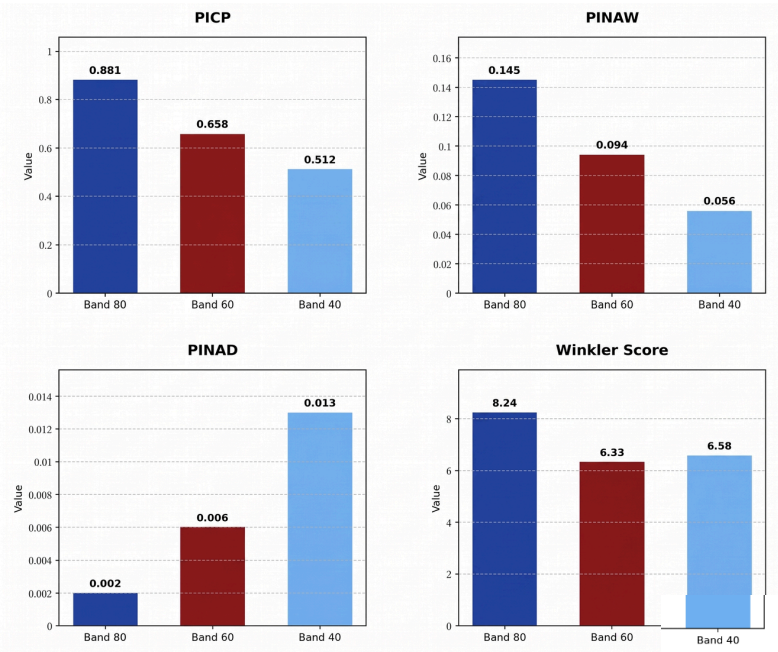
05. Simulation

■ Result 1 – Forecast Evaluation



- **PICP**

  In all quantile bands, the actual PICP exceeded the nominal coverage level
  → indicating that the prediction intervals secured demand coverage beyond the target level

- **PINAW / PINAD**

  PINAW (efficiency) and PINAD (reliability) exhibit an inverse relationship, preventing band selection based on a single metric

- **Winkler Score**

  Winkler Score applied as the final criterion by simultaneously reflecting interval width and deviation penalty

⟶ **Final conclusion**

Band 60, yielding the lowest overall Winkler Score, identified as the optimal forecasting interval satisfying both economic efficiency and reliability

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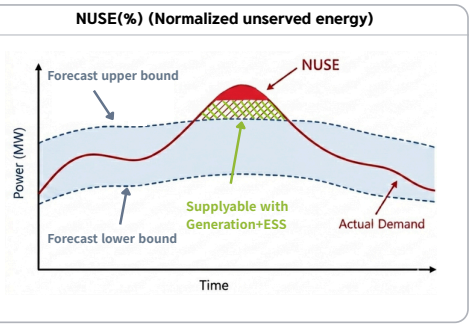
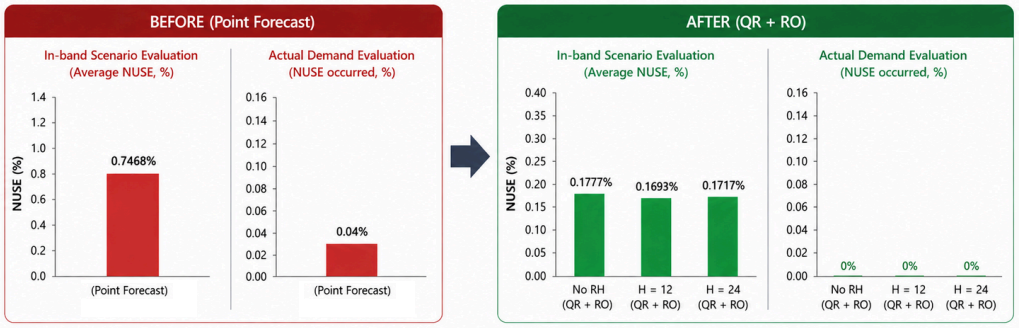
05. Simulation

■ Result 2 – Variability Control





- **Definition**

  Normalized index of annual unserved energy

- **Formula:**

$$\text{NUSE}(\%) = \frac{\text{Total unserved energy}}{\text{Total Demand}} \times 100\%$$

- **Point Forecast**

  – Reliance on a single forecast value leading to insufficient reserve procurement

  – Immediate outage (NUSE) occurrence under forecast errors

- **QR+Robust**

  – Preparation for worst-case scenarios based on QR forecasting

  – Stable supply-demand balance achieved even under actual demand fluctuations

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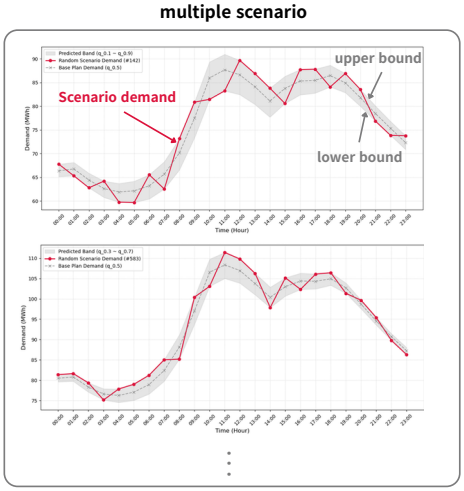
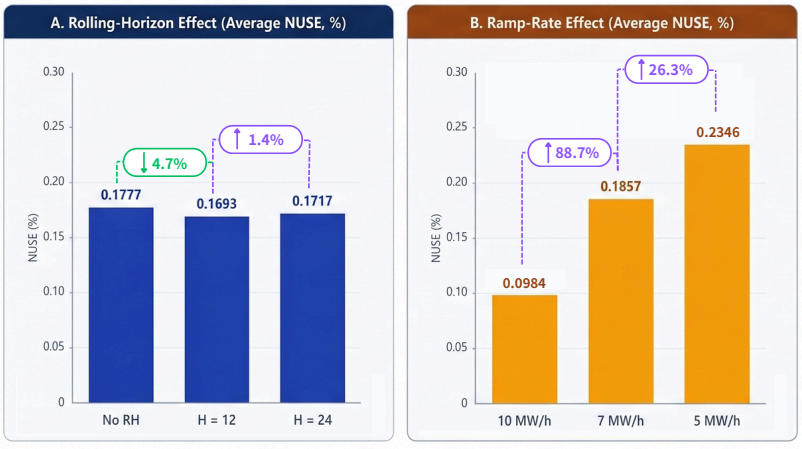
05. Simulation

■ Result 3 – Evaluation of Robustness under Scenario-based Testing



Each scenario composed solely of the upper (q0.9) and lower (q0.1) bound values of the forecast interval

→ representation of the most extreme demand realizations within the predicted range.



- Minimum NUSE at H = 12.
- Increase in NUSE due to reduced generator flexibility under lower ramp rates.

- Increase in NUSE due to reduced generator flexibility under lower ramp rates.

⟶ **Ramp rate is the dominant factor affecting robustness.**

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6. Conclusion

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06. Conclusion

■ **Summary**

- Applied quantile regression and robust optimization to handle demand variability and forecast uncertainty in EMS scheduling. Reserve was secured within the forecast interval, and rolling horizon operation eliminated unserved energy under uncertain demand.

■ **Suitable Applications**

- Effective for large-scale loads with high demand variability (railway stations, data centers, and EV charging hubs.)

■ **Limitations**

- EMS framework: does not yet include unit commitment(UC) constraints or detailed generator characteristics.
- Simulation: generator and ESS models were simplified, so results may differ from real-system operation.

■ **Future Work**

- Incorporate UC constraints and realistic generator characteristics into the EMS framework.
- Extend the simulation with detailed component models and field-level data for higher fidelity.

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Thank you

충북대학교
CHUNGBUK NATIONAL UNIVERSITY

Consideration of Noise Canceling Using Electromagnetic Bone Conduction Device

2026/5/14

Wataru Miyagoshi*, Wataru Kitagawa,
Nagoya Institute of Technology

[1]

Contents

- Overview of Research
- Measurement
  - Inverting amplifier circuit
  - Reduction requirements
- Conclusion

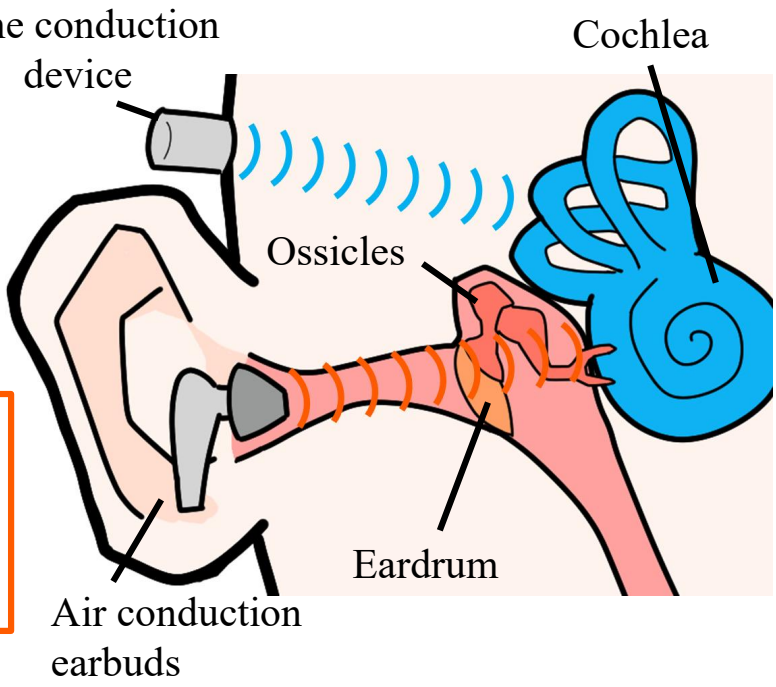
Research Background

Bone conduction

Skull vibrations
→Cochlea

Air conduction

Air vibration
→Ear canal →Ear drum
→Ossicles →Cochlea



- Works even with ear damage
- Hear sounds without blocking your ears

Research Subject and Object

Subject

- Can't block out noise
- Standard control methods do not work

⇩

Object

- Check the noise canceling effect and requirements
- Implementation of noise cancellation

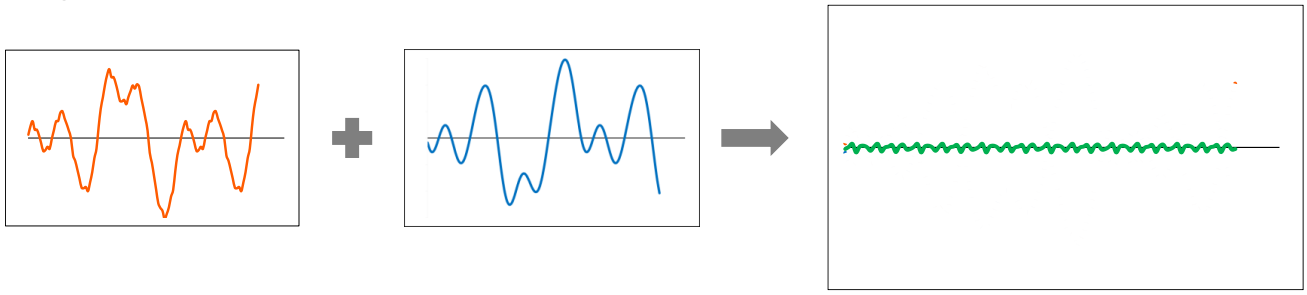
Noise Canceling Method

PNC:Passive noise cancellation

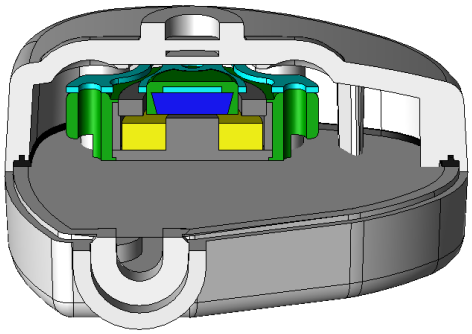
Directly reduce incoming noise using earplugs or earpads.

ANC:Active noise cancellation

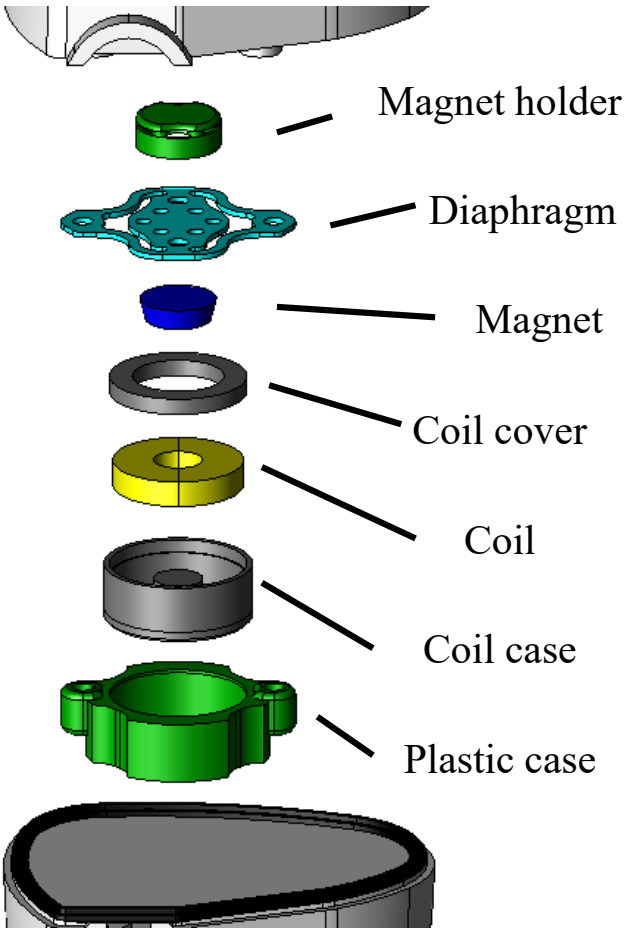
Reduce noise by generating a phase-inverted signal to cancel it out.



Structure

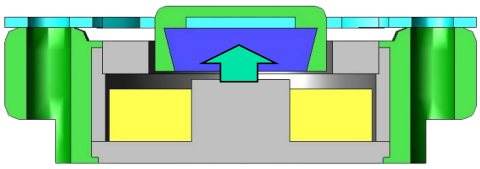


Parts	Material
Diaphragm Coil case Coil cover	SUS430
Magnet	NEOMAX-35AH
Coil	Copper
Magnet holder Plastic case Case	ABS543(Techno)



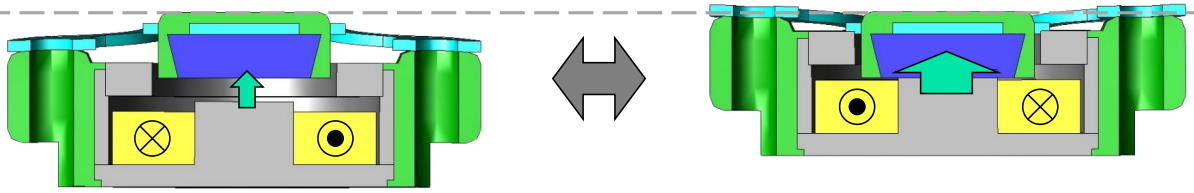
Operational Mechanism

Power off



Constant magnetic force
from magnet flux

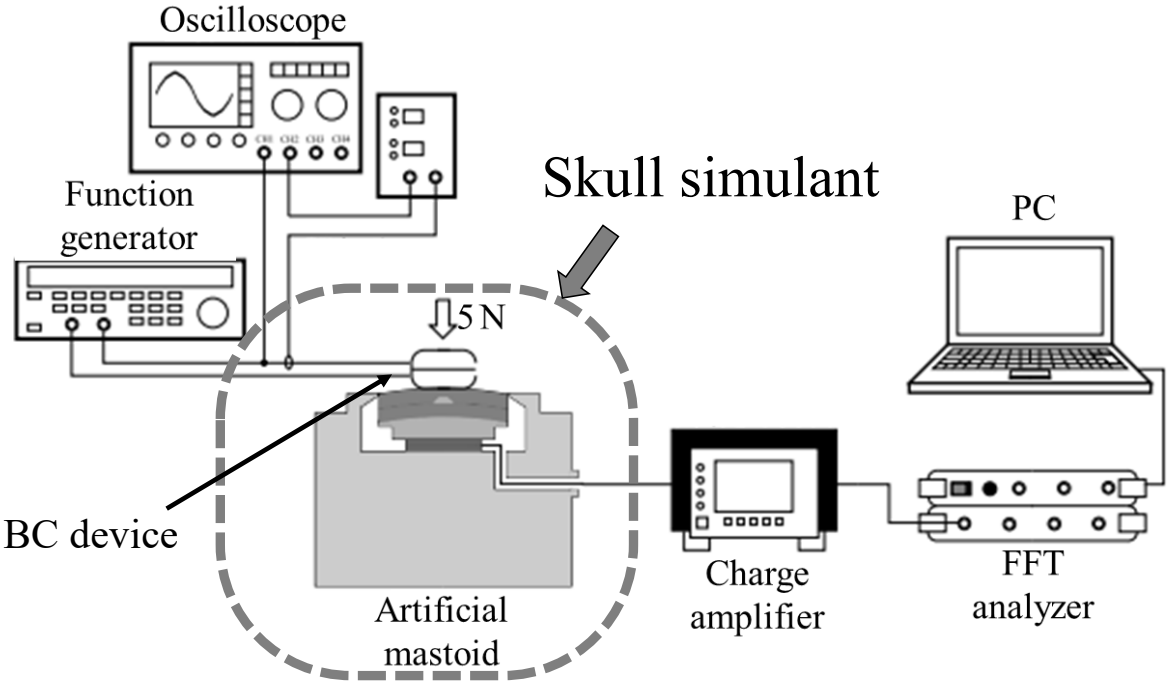
Current flow



Magnet flux
+
Coil flux

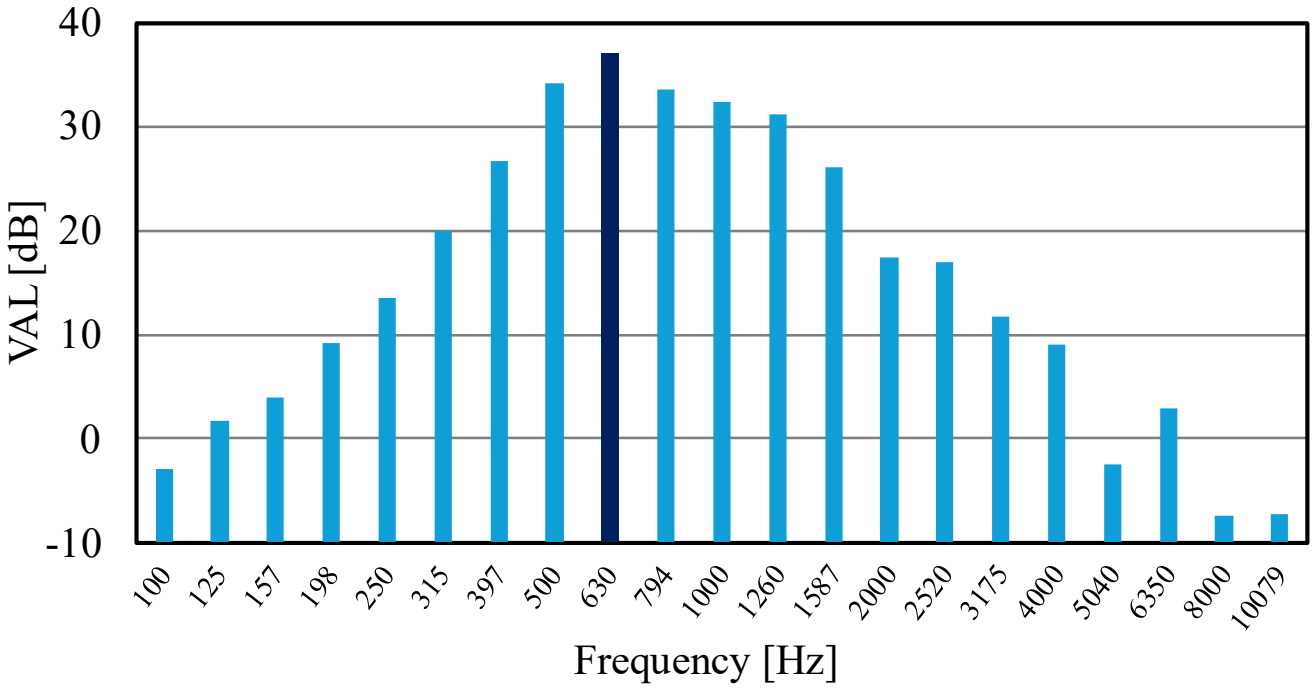
→ Change magnetic force between the magnet and coil case → Vibration

Measurement of actual device output



- Apply sine wave voltage
- Measure frequency response using FFT analyzer

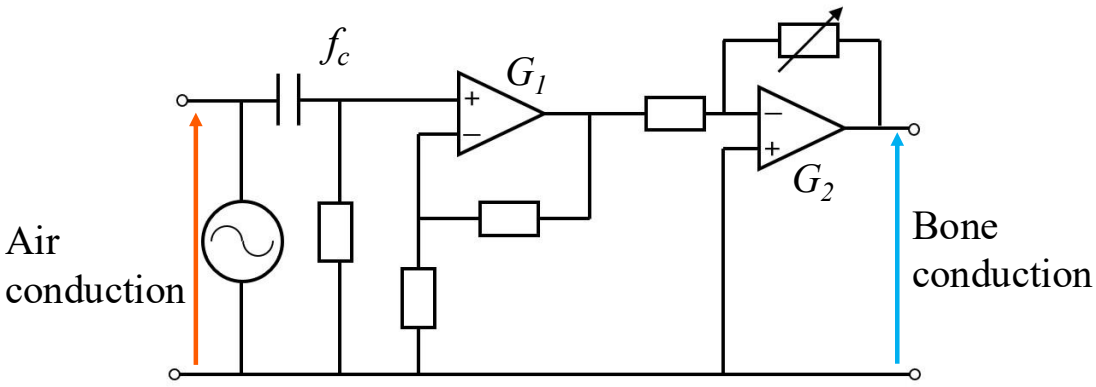
Actual device output



- Output characteristics with a peak at 630 Hz
- Resonance point identified at 630 Hz via structural analysis

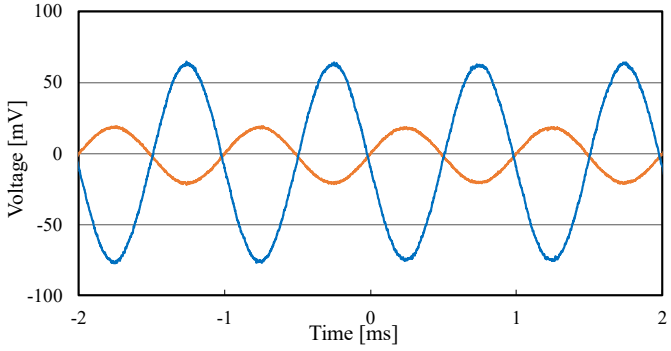
Contents

Inverting Amplifier Circuit Configuration

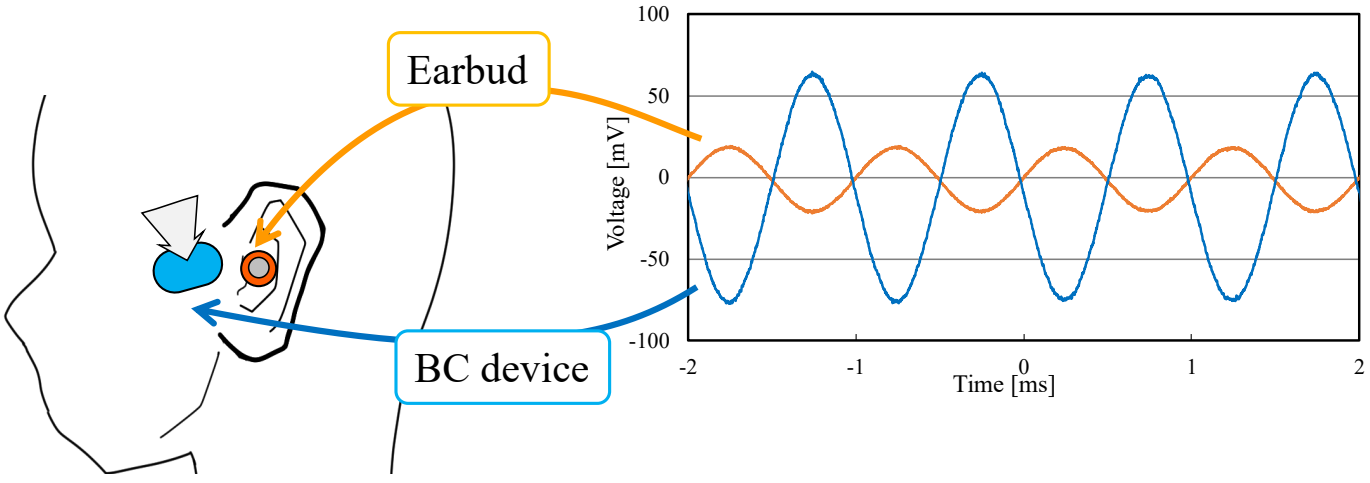


Cut-off frequency	f_c	16.9 Hz
Gain	G_1	23
	G_2	0 ~ 2.5

Adjust using variable resistor



Reduction via Inverted Signal



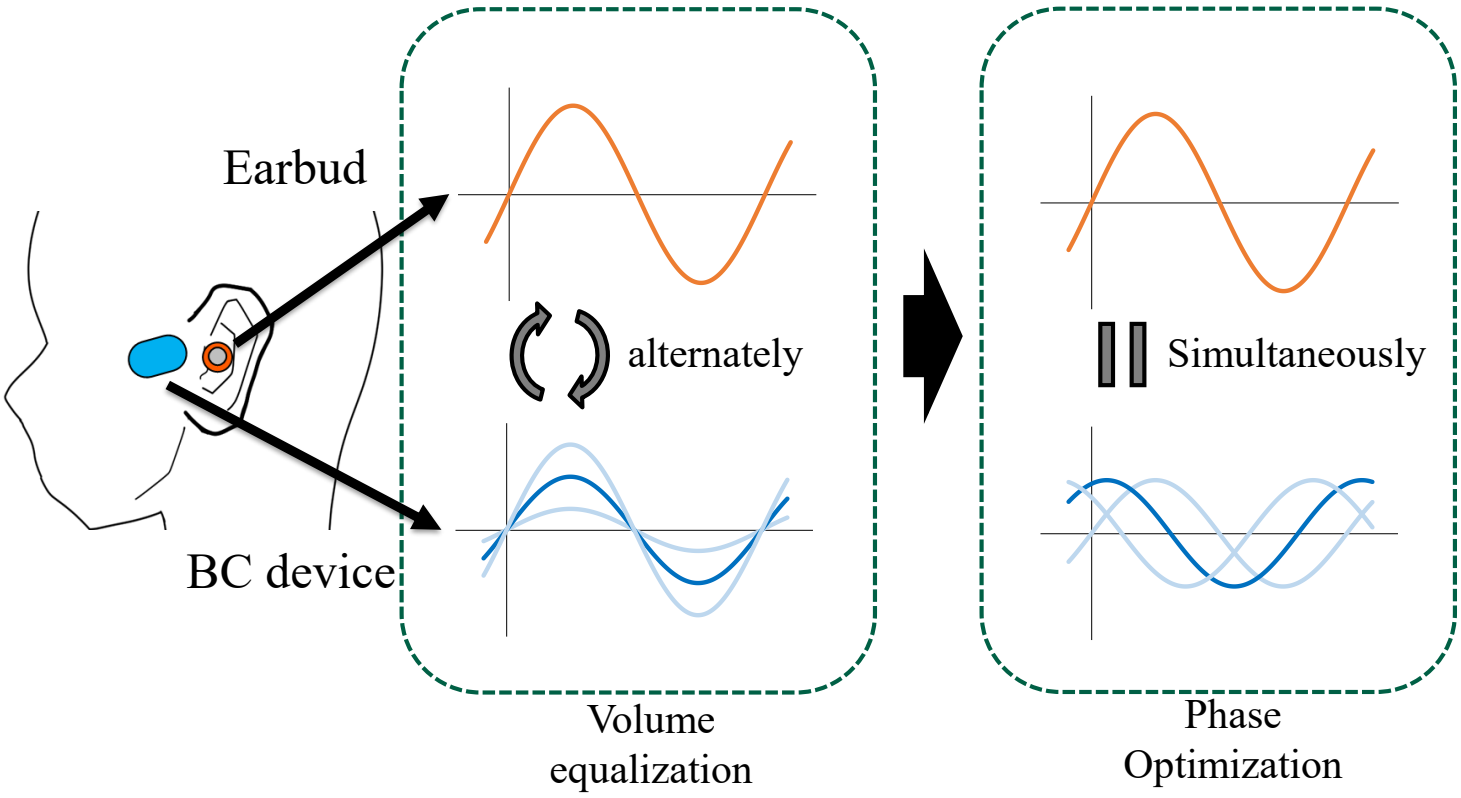
	500 Hz	1000 Hz	2000 Hz
A	△	○	×
B	×	△	—
C	△	×	—

○ : Effective reduction
△ : Slight change
× : No noticeable change

Contents

- Overview of Research
- Measurement
  - Inverting amplifier circuit
  - Reduction requirements
- Conclusion

Measurement Procedure

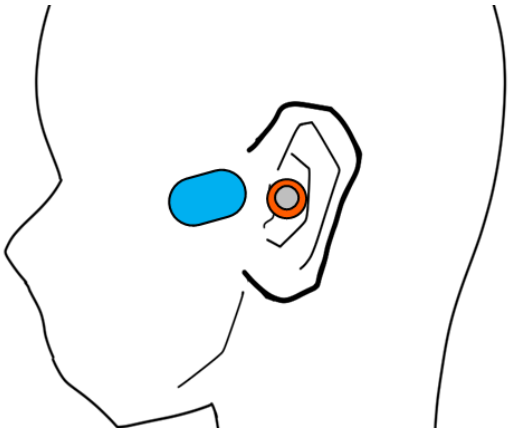


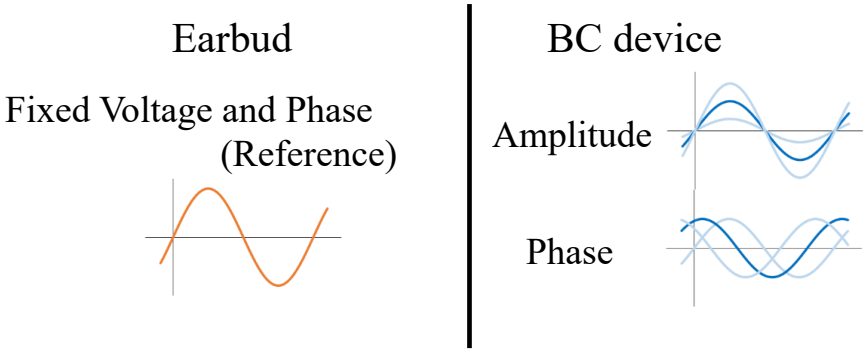
Measurement Procedure

1. Wearing both earbud and BC device on the left ear.

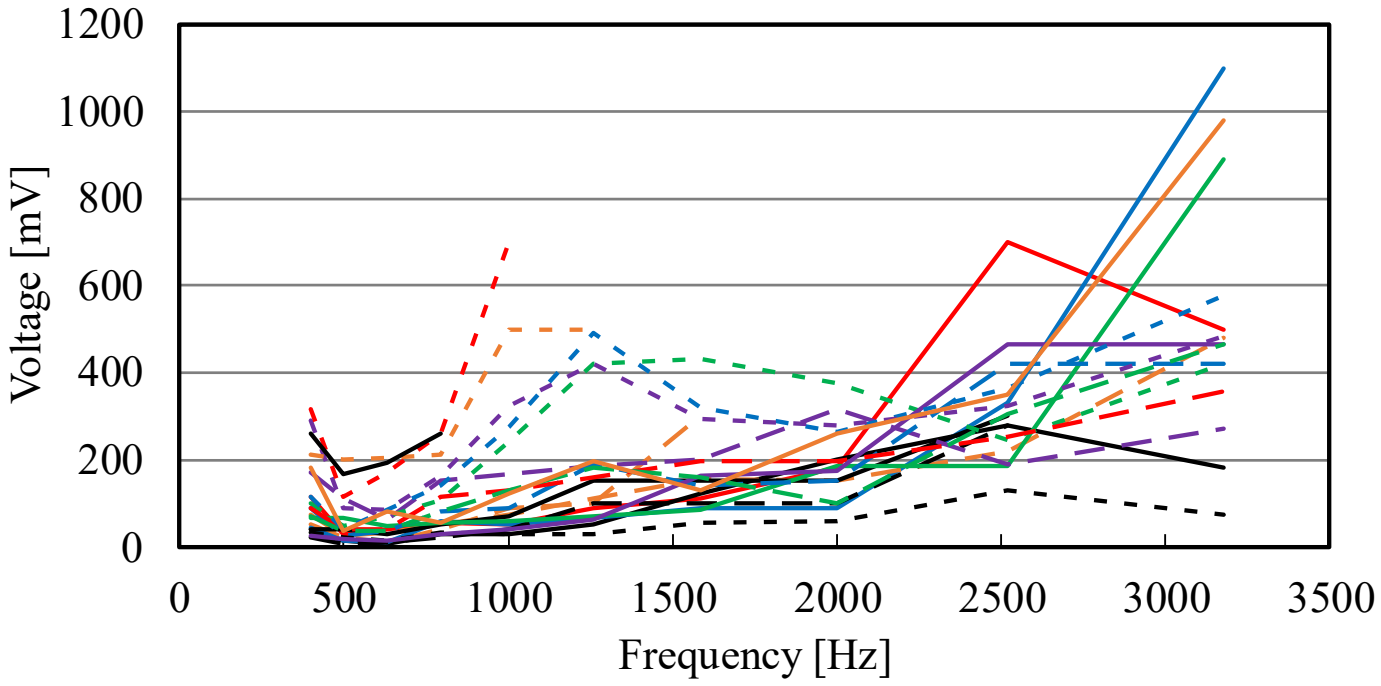
2. Play sound alternately and adjust the BC voltage to match the volume.

3. Play sound simultaneously and adjust the BC phase to minimize the volume.



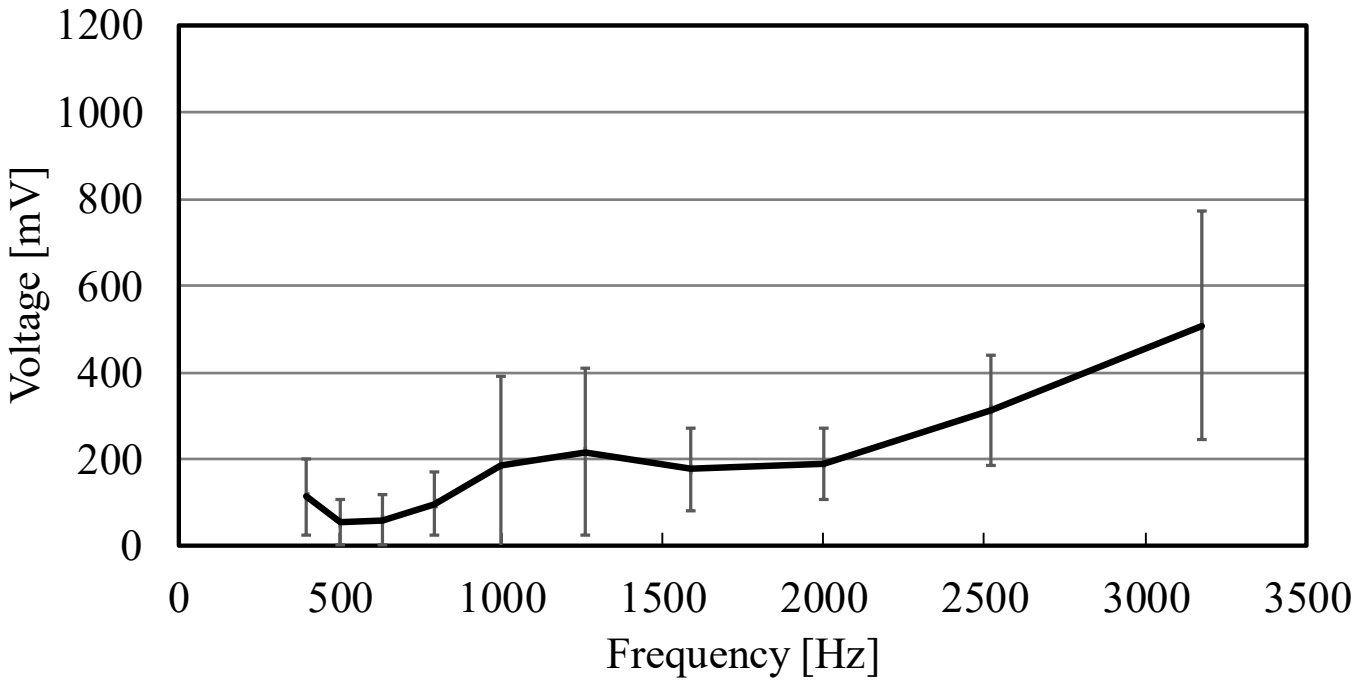


Equally Perceived Voltage



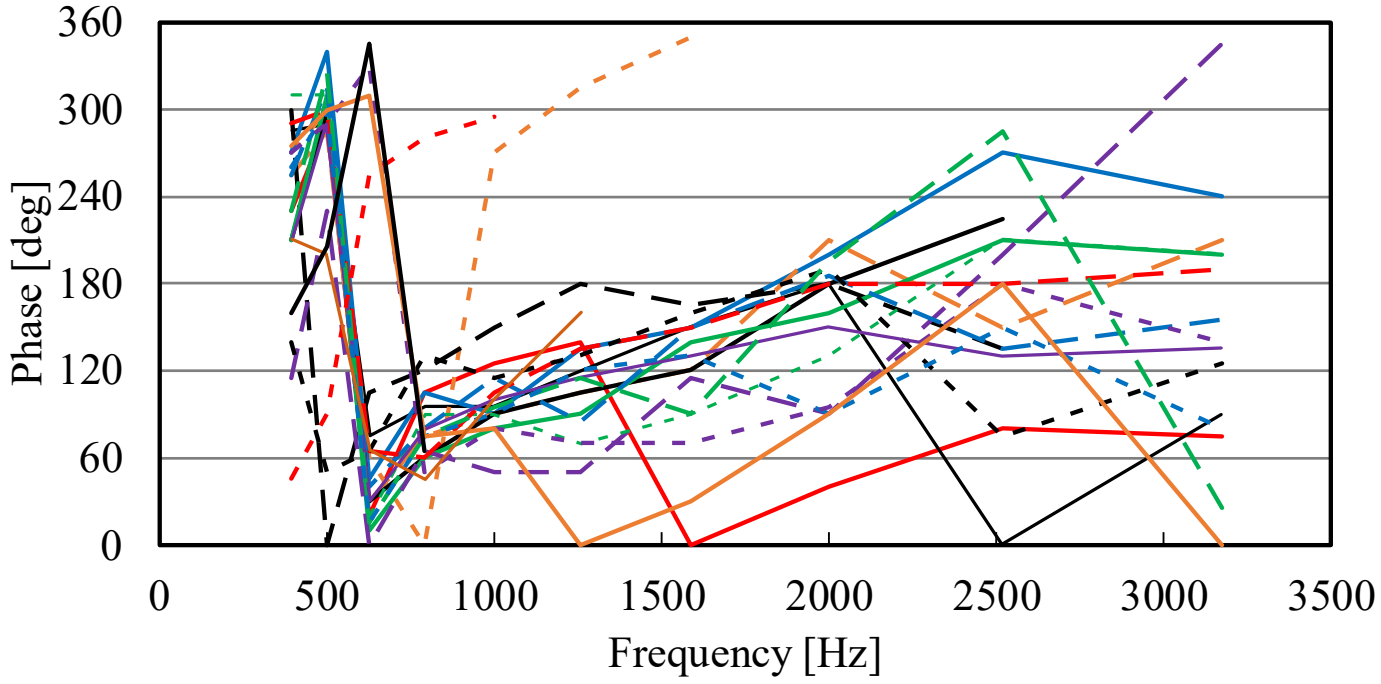
■ Significant voltage increase around 1000 Hz and 3000 Hz
→Higher variability

Equally Perceived Voltage



- Higher variance around 1000 Hz and 3000 Hz
- Lowest voltage at 630 Hz

Optimal Phase for Reduction



- Shape decrease in 500 ~ 700 Hz
- Full range phase variation around 3000 Hz

Measurement Result

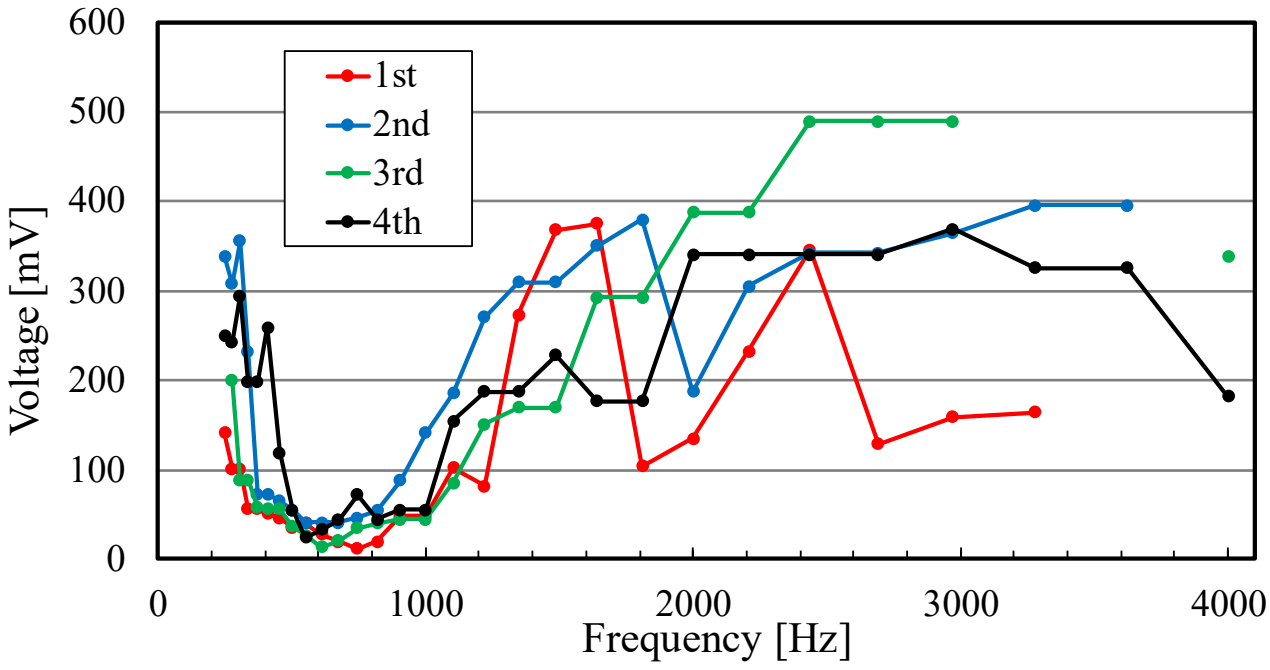
- High voltage and phase variability around 1000 and 3000 Hz

- Fit of the earpiece affects bone conduction volume
- Degradation of BC sound quality above 2000 Hz

17/21 subjects perceived sufficient reduction
with the 397 ~ 2520 Hz range

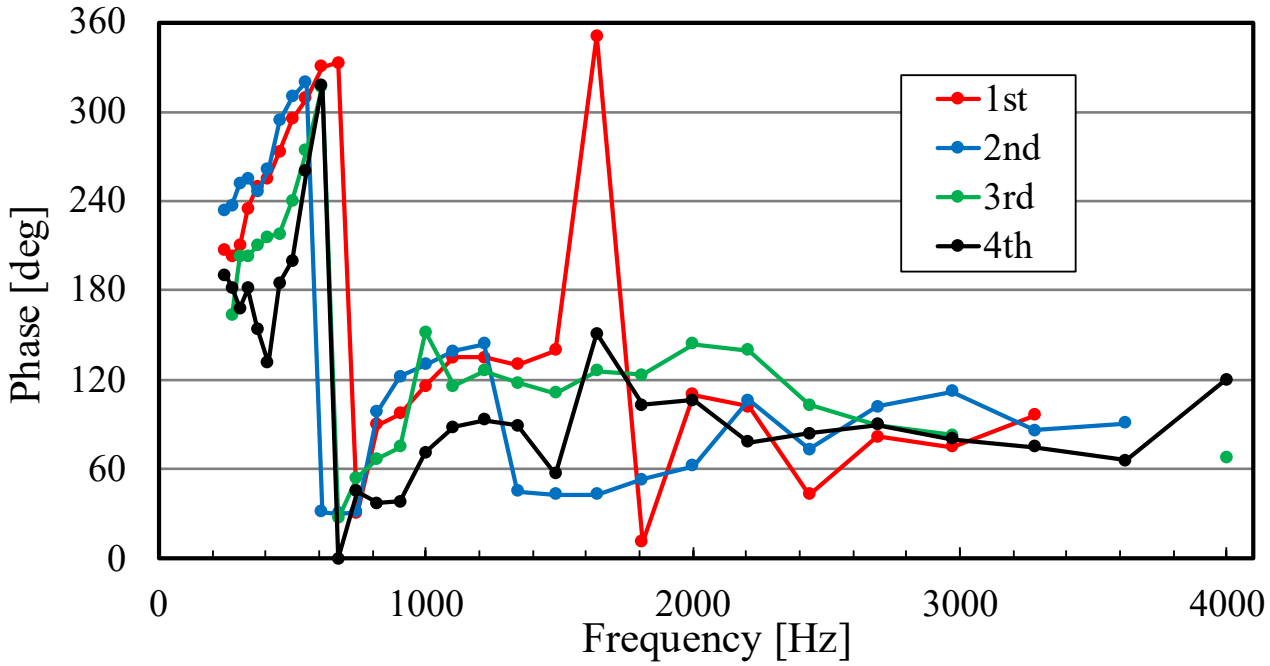
⇨ Variability due to fitting

Equally Perceived Voltage



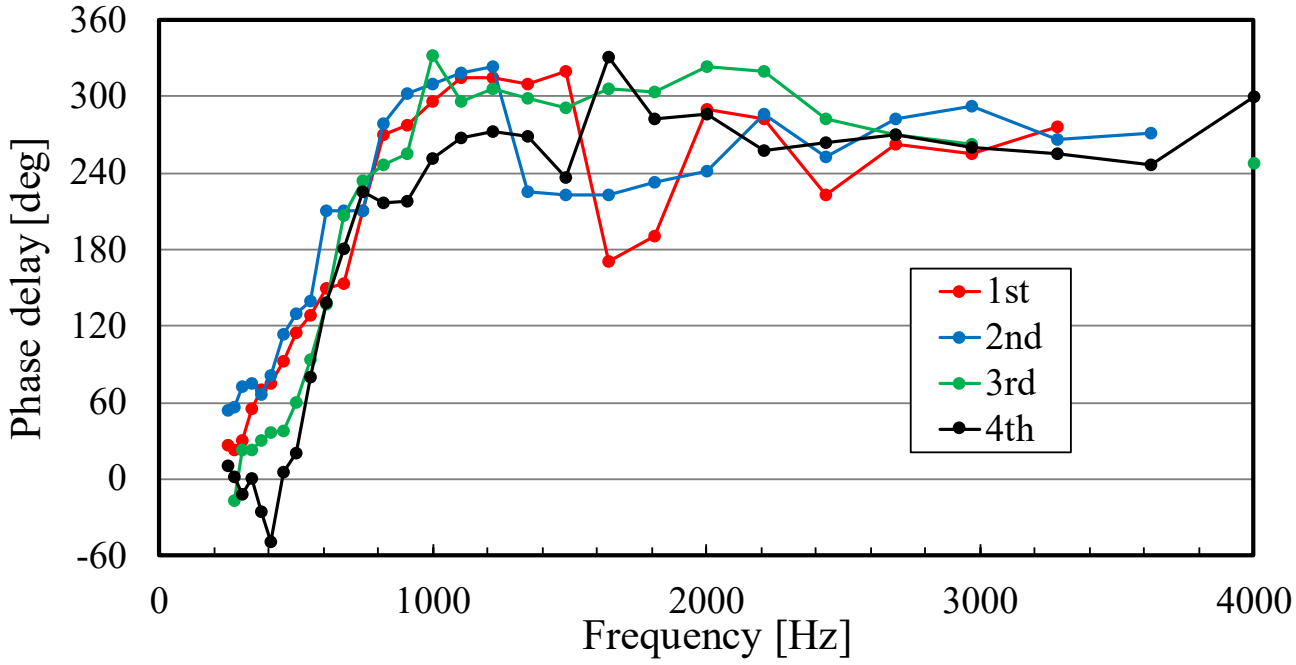
- Lowest voltage at 630 Hz
- Highly variation above 2000 Hz

Optimal Phase for Reduction



- Shape decrease in 500 ~ 700 Hz
- Low variability except around 1600 Hz

Estimated BC Device Delay



- Shape decrease in 500 ~ 700 Hz
- Full range phase variation around 3000 Hz

BC Device Delay

BC sounds perception delay

Possible factor

- High inductive reactance component
- Slow vibration propagation in the skin
- Heavier transducer compared to earbuds
  →High mechanical impedance

Demerit

- Inability to handle
  high-frequency, non-periodic, impulsive noise

Conclusion

Object

- Implementation of noise cancellation

Result

- Effective for periodic noise
  - sufficient reduction with the 397～2520 Hz range
- BC sounds perception delay

Forward

- Check and reduce delay
- Improving output in the high-frequency range

Development of SSCB on the Train Auxiliary Power Supply(SIV) of Urban Railway

6th Joint University Students Workshop

Geonhui Hyeong

Chungbuk National University
Electric Machine Drive Lab

충북대학교 CHUNGBUK NATIONAL UNIVERSITY
Electric Machine Drive Lab

OUTLINE

❖ Types of urban railway vehicles

K-AGT(rubber-tired system)

- Korea's first driverless operation system
- Busan Metro Line 4 (rubber-tired system), 102 cars

Incheon IAT

- Incheon Airport Railroad
- Rubber-tired light rail transit, 6 cars
- Fully automated driverless operation using ATO/ATP

Sillim Line

- Yeouido to Seoul National University Station

Smart Monorail

- Taejongdae Monorail

Medium-sized Monorail

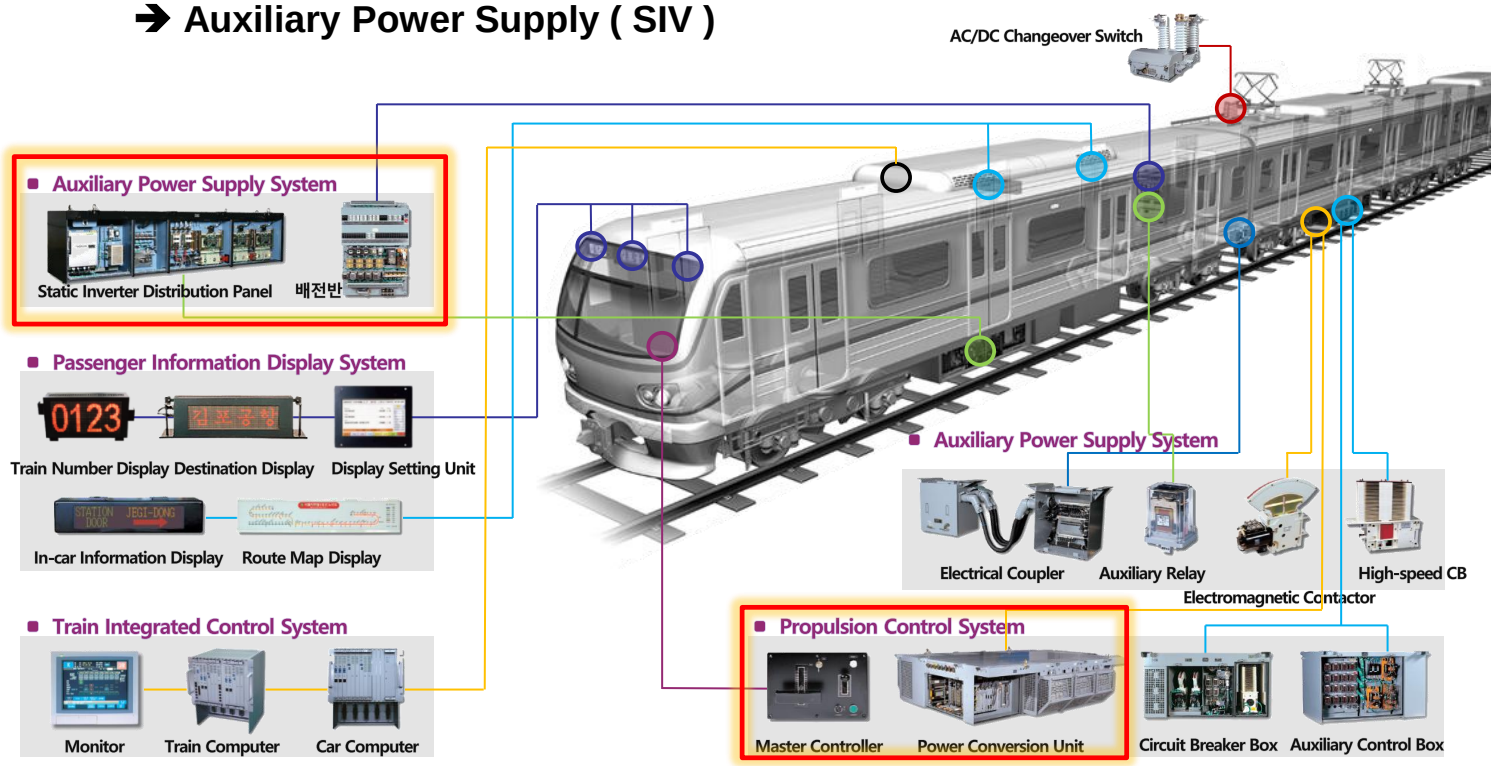
- Daegu Transportation Corporation Line 3, 84 cars
- Signaling: Fully automated driverless operation using ATP/ATO

❖ Major electrical equipment for railway vehicles

► Propulsion & Service Power Converters

➔ **Propulsion Control Unit**

➔ **Auxiliary Power Supply (SIV)**



❖ Recent Need for SSCB Development

[*] https://developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories/

1 Introduction

❖ Recent Need for SSCB Development

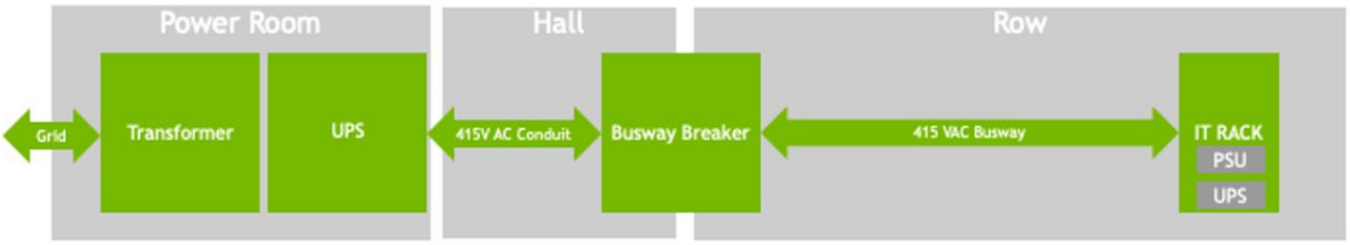


Figure 1. Current data center power architecture

The 800 VDC revolution

NVIDIA 800 VDC architecture addresses these challenges through a holistic redesign. NVIDIA is collaborating with the data center power ecosystem on the innovations and changes that will be necessary to realize this concept.

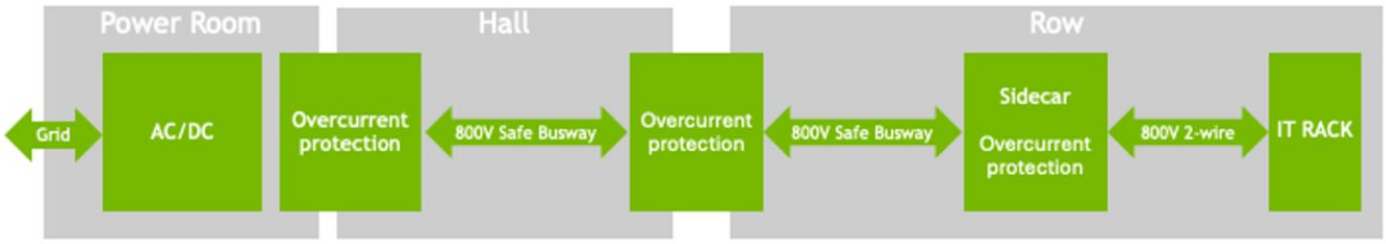


Figure 2. NVIDIA 800 VDC architecture minimizes energy conversions.

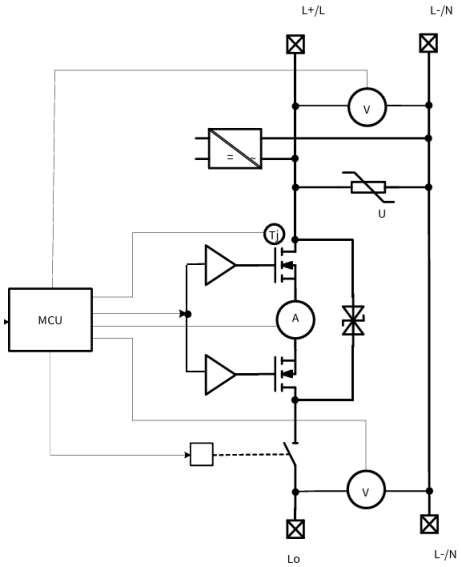
[*] https://developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories/

OUTLINE

2 Short-Circuit Current Sensing

❖ Short-Circuit Current Sensing Method

- ▶ It immediately turns off the SSCB semiconductor switch when the fault current exceeds the threshold.
- ▶ Short-circuit current sensing can be implemented using the following methods.
  - ✓ Desaturation Detection, TMR Current Sensor, Hall-effect Sensor
  - ✓ Shunt Resistor sensing, Rogowski Coil

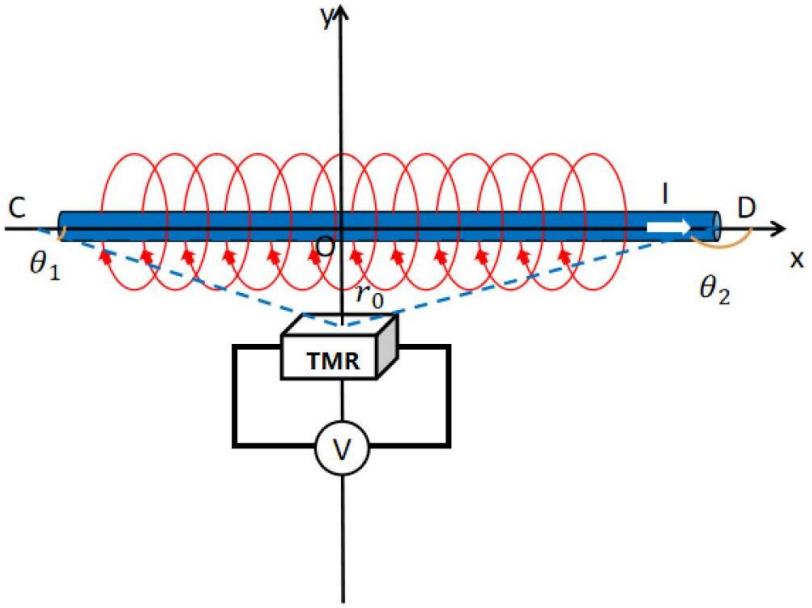


< MCU Current sensing block diagram >

[*] https://www.infineon.com/application/solid-state-circuit-breaker

❖ TMR Current Sensor

- ▶ TMR current sensors offer galvanic isolation and high bandwidth.
- ▶ Their performance can be affected by temperature variation, external magnetic fields, and sensor placement.
- ▶ Temperature compensation and magnetic shielding are required.

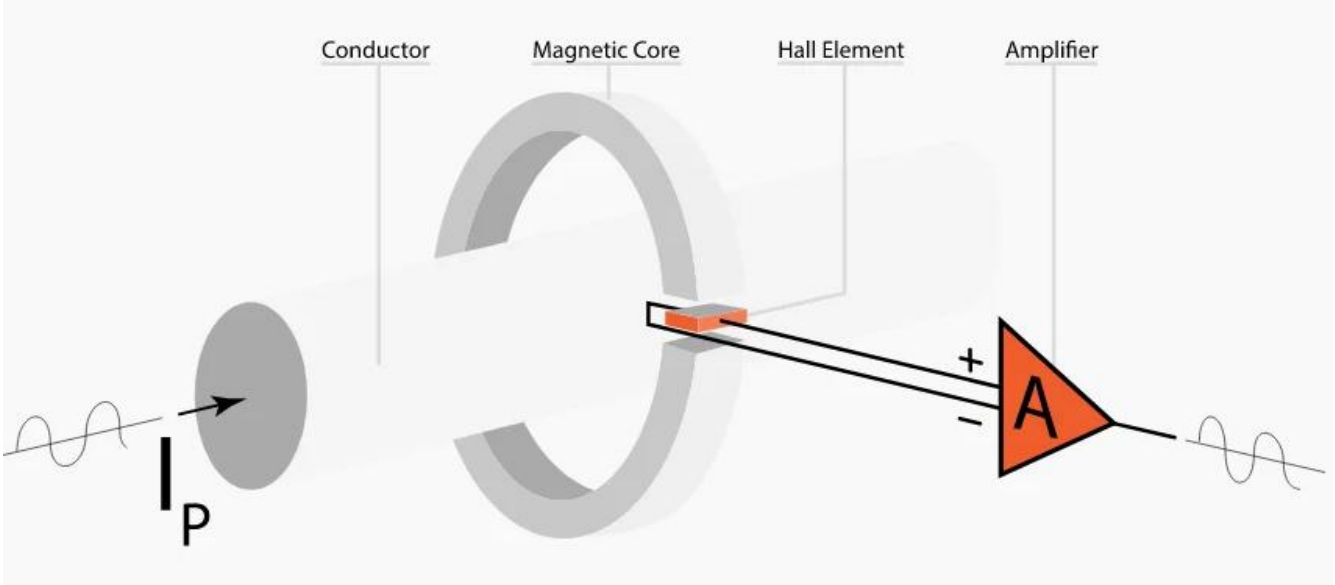


< TMR Current sensor >

[*] https://pmc.ncbi.nlm.nih.gov/articles/PMC11857788/

❖ Hall-effect Sensor

- ▶ It measures current by detecting the magnetic field generated around the current path using the Hall effect.
- ▶ Hall-effect sensors provide galvanic isolation, but magnetic saturation and limited bandwidth make them less suitable for fast SSCB fault detection.

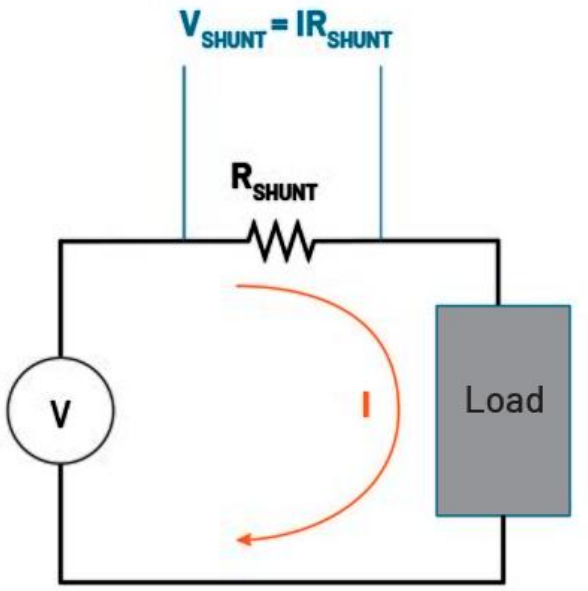


< Hall-effect sensor >

[*] https://www.allaboutcircuits.com/technical-articles/hall-effect-current-sensing-open-loop-and-closed-loop-configurations/

❖ Shunt Resistor sensing

- A shunt resistor detects fault current by measuring the voltage drop across a low-value resistor inserted in the current path.
- It is simple and fast, but causes power loss, heat generation, and requires additional isolation in high-voltage SSCBs.

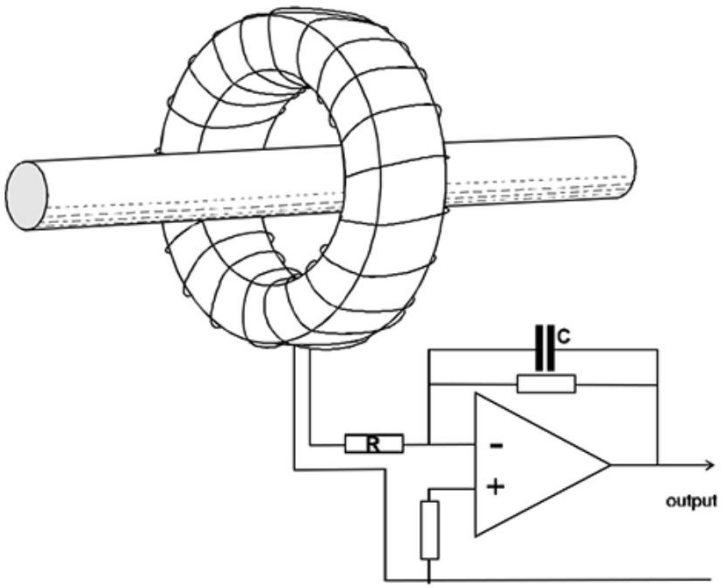


< Shunt resistor sensing >

[*] https://www.tek.com/en/blog/measuring-current-using-shunt-resistors?

❖ Rogowski coil

- A Rogowski coil measures the current change rate $di/dt$from the magnetic field around a conductor and integrates it to obtain current.
- It offers wide bandwidth and galvanic isolation, but cannot directly measure DC current and requires an integrator.

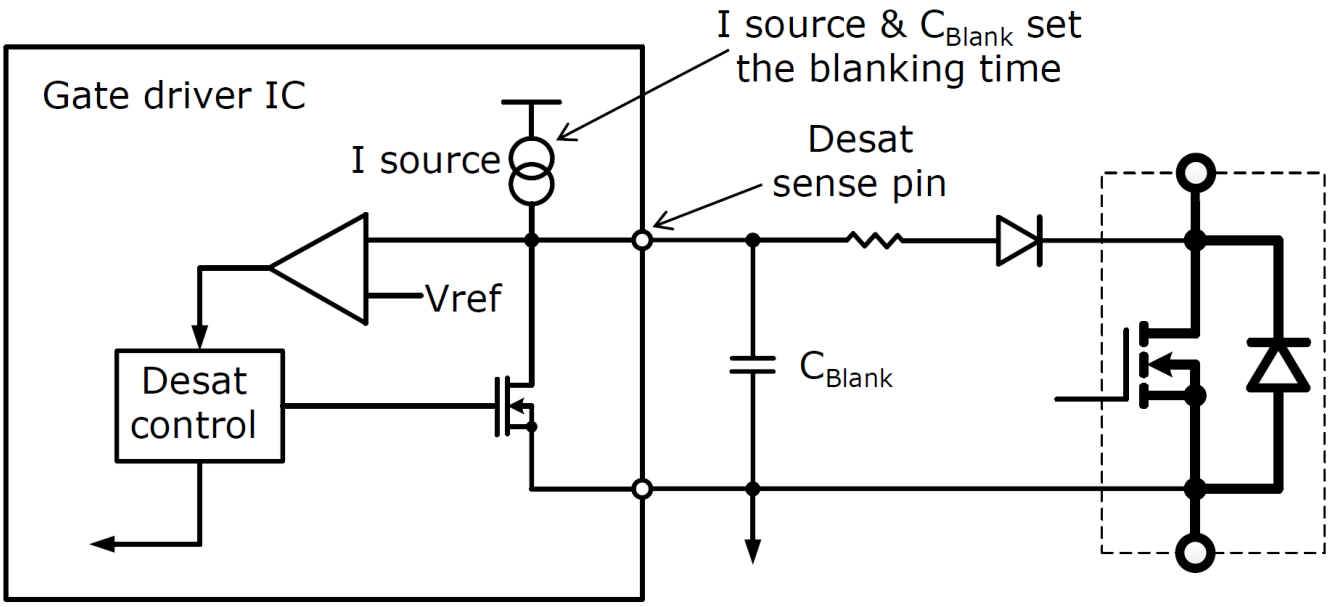


< Rogowski coil sensing >

[*] https://www.rocoil.co.uk/rogowski-coils/

❖ Desaturation Detection

- DESAT is a gate-driver-based protection method that detects short-circuit faults by monitoring the voltage rise across a conducting semiconductor switch.
- It is suitable for SSCB protection because it enables very fast fault detection and can be directly implemented in the gate driver circuit.



< infineon's DESAT Circuit >

[*] https://www.infineon.com/product-information/power/gate-driver-ics/eicedriver-enhanced

❖ Desaturation Detection Gate IC' Time Delay

- Even after DESAT detection, soft turn-off causes a delay before complete interruption.
- Therefore, both semiconductor short-circuit withstand capability and gate-driver turn-off delay must be considered.

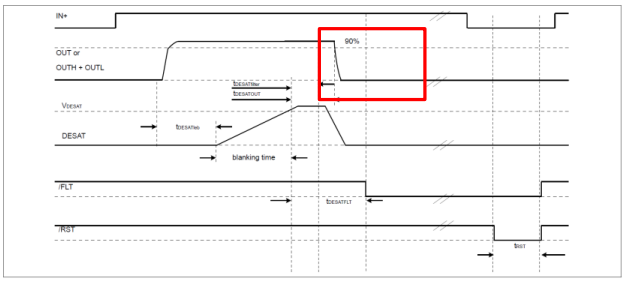


Figure 12 DESAT hard off behavior

The Figure 13 show the soft off behavior.

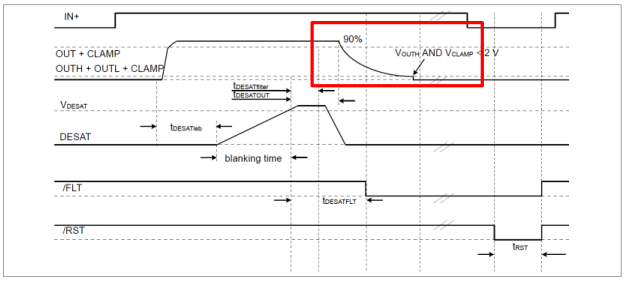


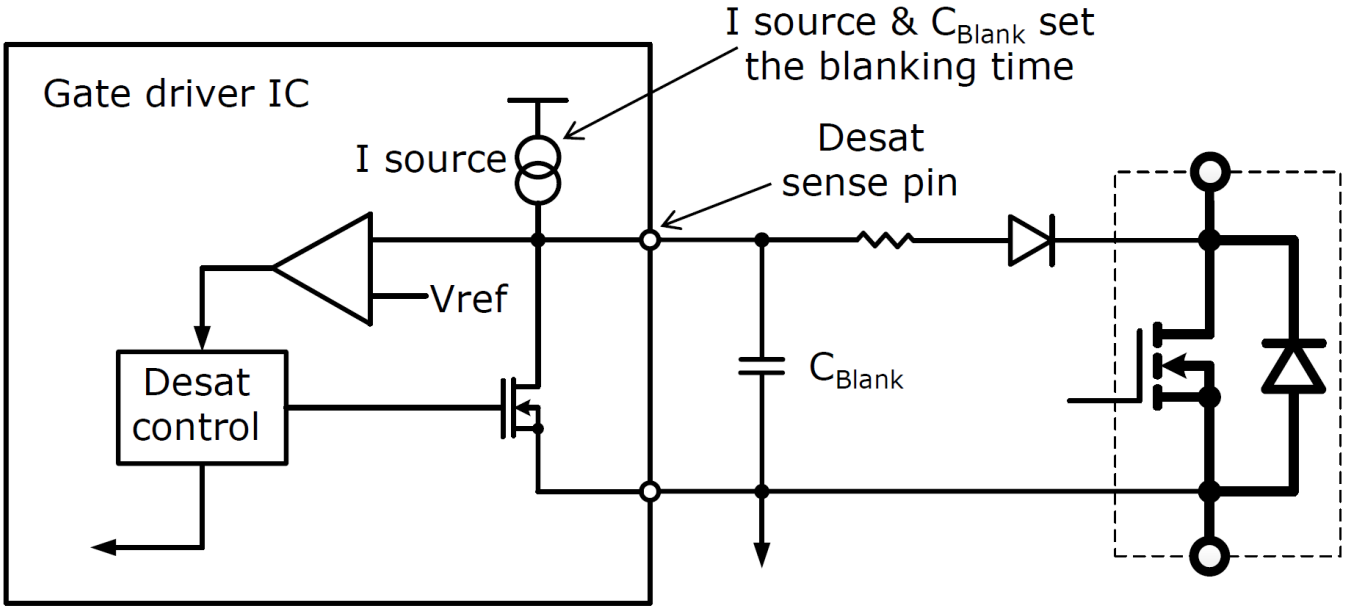
Figure 13 DESAT soft off behavior

< Differences in DESAT Behavior of Gate Driver ICs >

[*] https://www.infineon.com/product-information/power/gate-driver-ics/eicedriver-enhanced

❖ Desaturation Detection principle

- A DESAT circuit detects a short-circuit fault by monitoring the rise of V_{DS}or V_{CE}while the switch is ON.
- During normal conduction, the switch voltage is low, but under a short-circuit fault, high current causes the voltage to rise and triggers DESAT detection.

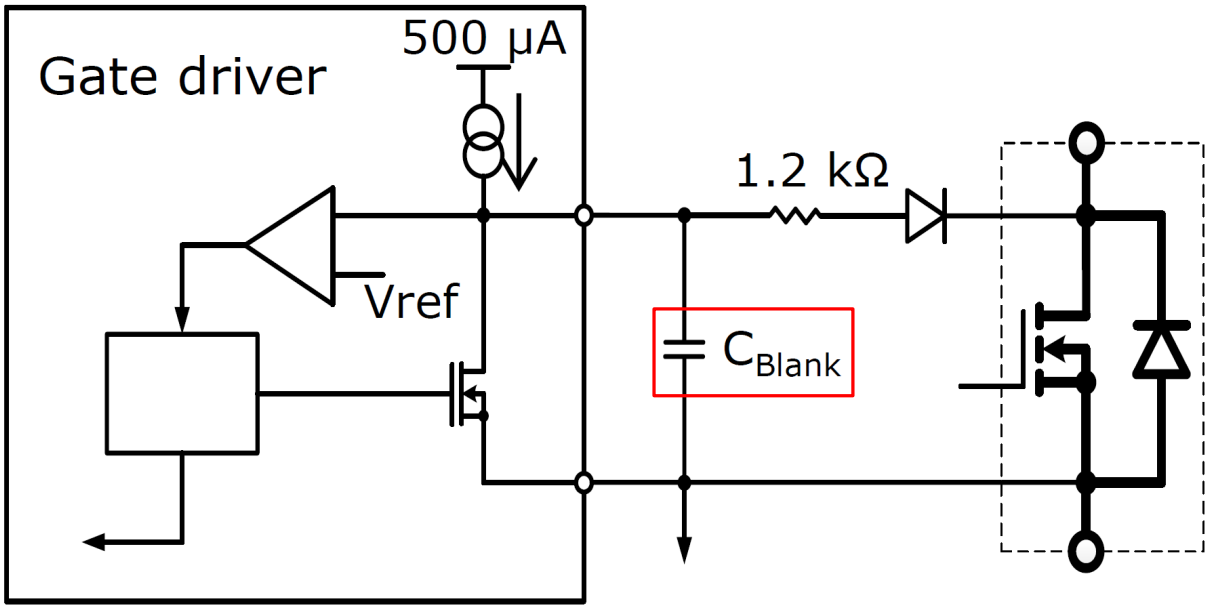


< infineon's DESAT Circuit >

[*]

❖ Desaturation Detection principle detail

- The blanking capacitor sets the DESAT blanking time to prevent false detection right after turn-on.
- During normal turn-on, V_{DS}decreases, so $C_{Blank}$is not fully charged and the DESAT pin voltage stays below V_{ref}.

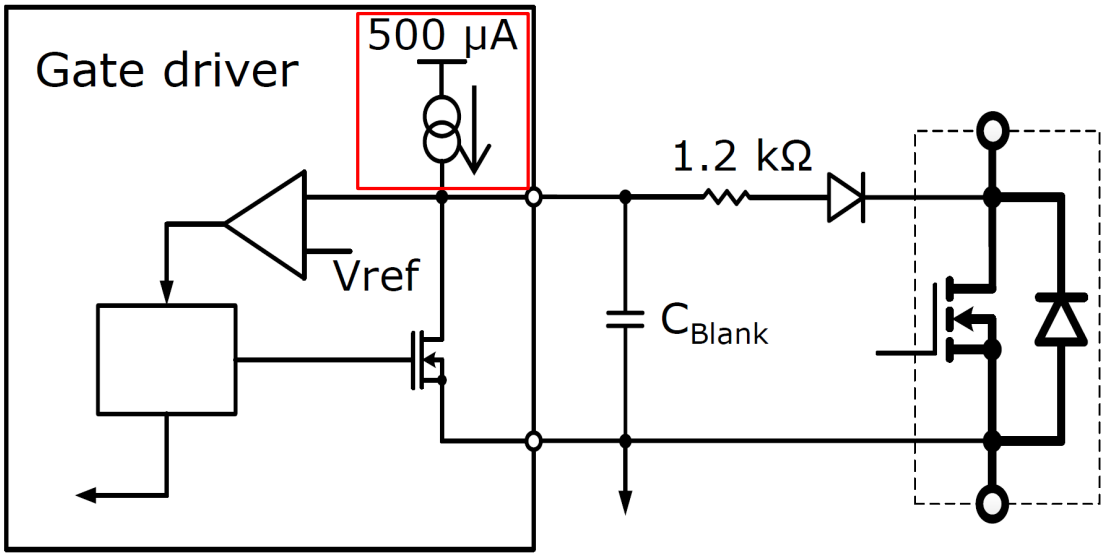


< infineon's DESAT Circuit >

[*]

❖ Desaturation Detection principle detail

- During a short-circuit fault, V_{DS}remains high even when the MOSFET is ON due to the large fault current.
- The DESAT current cannot discharge toward the drain, so C_{Blank}keeps charging.
- V_{DESAT} exceeds V_{ref} ,the gate driver detects fault and turns off the switch.



< infineon's DESAT Circuit >

[*]

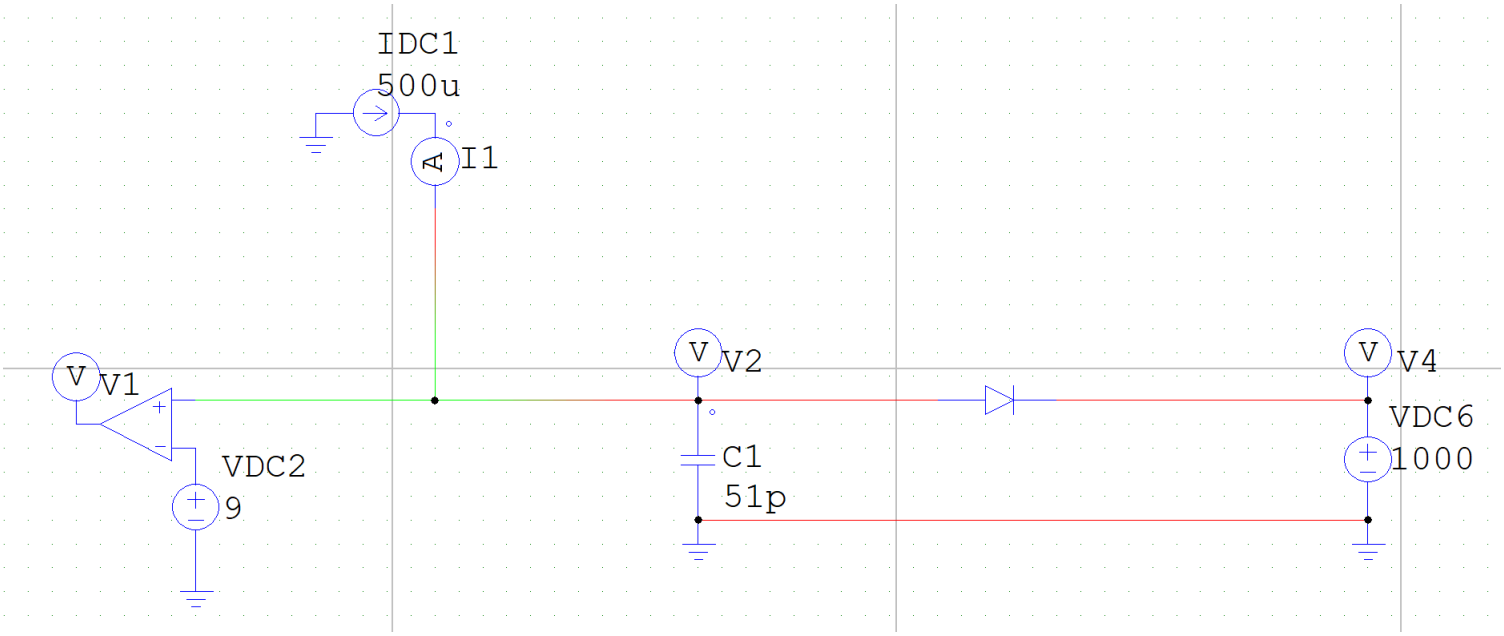
❖ SiC MOSFET Short-circuit capability

- For Infineon CoolSiC MOSFETs, the short-circuit withstand capability varies depending on the device series, but it is typically around 2 µs.
- Therefore, short-circuit protection must be completed within 2 µs.
- For the gate driver IC shown in the previous material, the internal current source is **500 µA**, and the $V_{ref}$of the internal comparator is **9 V**.
- The short-circuit protection operating time is calculated as follows.
  - ✓ $t_{DESATBLANK} + t_{DESATOUT} < t_{SC} = 2$ [µs]
  - ✓ $t_{DESATBLANK} = \frac{C_{DESAT} * V_{DESATth}}{I_{DESAT}} = \frac{51[pF]*9[V]}{500[\mu A]} = 0.918[\mu sec]$
- $t_{DESATOUT}$ varies depending on whether **soft turn-off** or **hard turn-off** is used.

[*]

❖ DESAT Simulation circuit

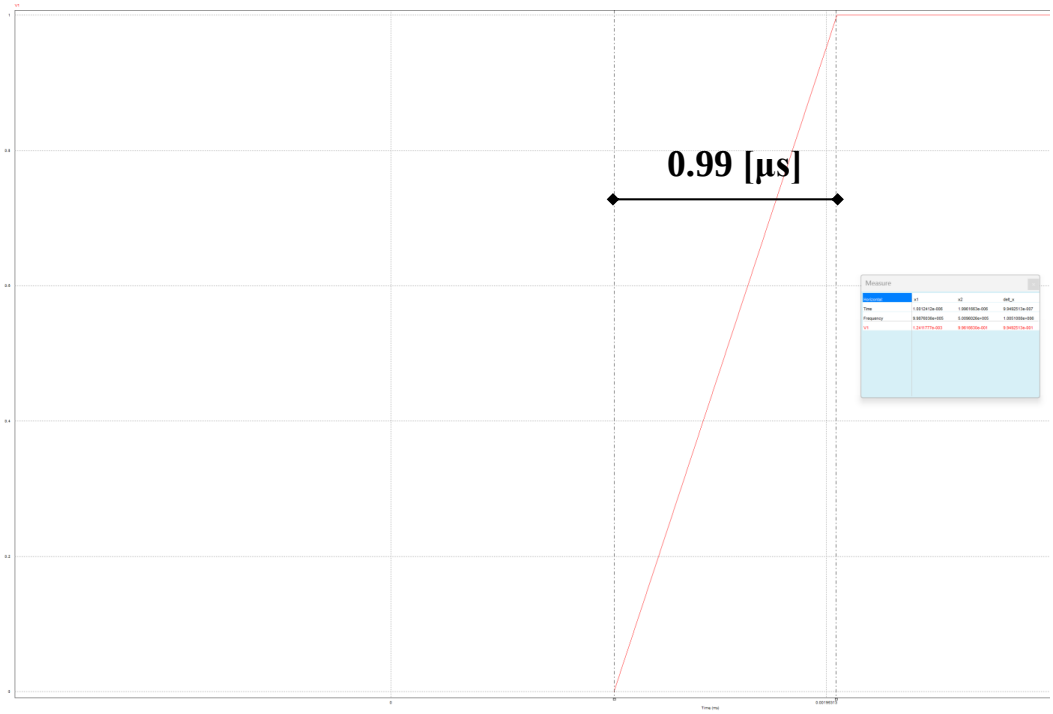
- ▶ Simulation Circuit for DESAT Time Verification



[*]

❖ DESAT Simulation result

- ▶ The signal output time is 0.99 [μs].
- ▶ Although there is a slight difference from the calculated value, the simulation shows a similar result.



[*]

❖ Hard-off behavior time delay

- For hard turn-off, only the internally set delay time of **0.918 [μs]** to prevent false triggering and the gate IC internal delay of **350 [ns]** are considered.
- Assuming the voltage falls ideally, the operating time is calculated as follows
  - ✓ $t_{DESATBLANK} + t_{DESATOUT} = 0.918[us] + 0.350[us] = 1.268\ [us]$
- This satisfies the **2 [μs]** short-circuit withstand capability of the SiC MOSFET.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pulse suppression filter time	$t_{DESATfilter}$		250		ns	*1)*
Desaturation sense to out low delay	$t_{DESATOUT}$		350	430	ns	V_{OUT} = 90 %, C_{OUT} = 1 nF, *OUT* = *OUTH* + *OUTL* shorted, 1ED3322, 1ED3323

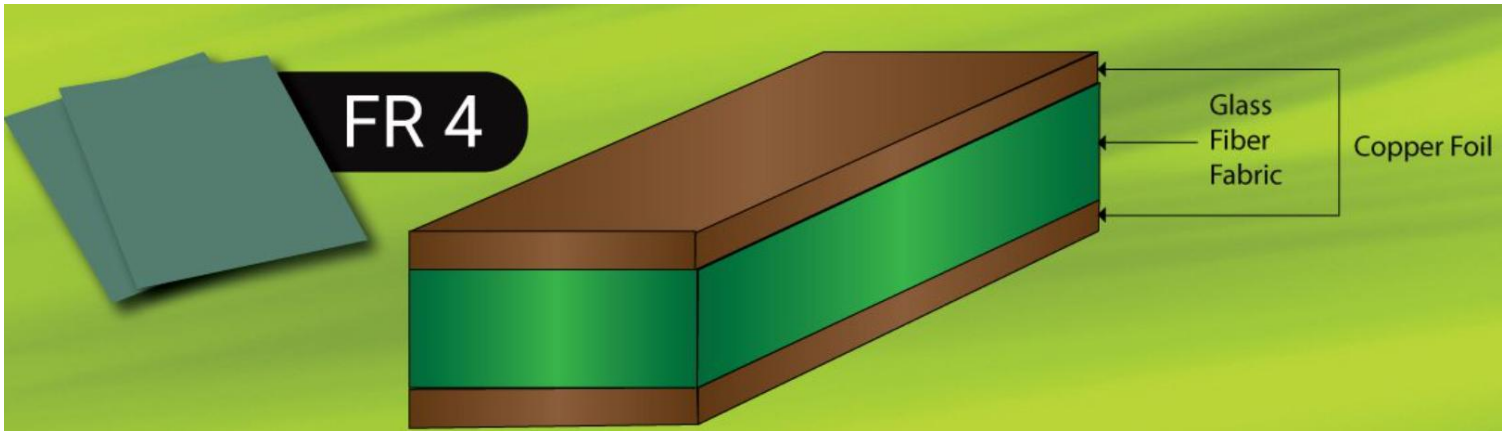
< Hard-off behavior in datasheet >

[*]

OUTLINE

❖ Considerations for PCB

- The input and output currents of the SSCB are several tens of amperes higher than those of signal lines.
- When high current flows through a PCB trace, I^2R loss occurs due to trace resistance, leading to temperature rise.
- Temperature rise in PCB traces can increase copper resistance and degrade insulation, FR-4 reliability, and solder-joint durability.



< PCB' Trace structure >

[*] https://www.globalwellpcba.com/

❖ PCB Trace Width

- As mentioned before, the PCB traces of the SSCB must be designed considering trace thickness and width according to the current level.
- The trace width was evaluated for a current level of 55 [A].
- The required trace width was calculated using DigiKey's Trace Width Calculator.

< Digikey' Trace width caculator >

[*] https://www.digikey.kr/ko/resources/conversion-calculators/conversion-calculator-pcb-trace-width

❖ PCB Trace Width Calculation with condition

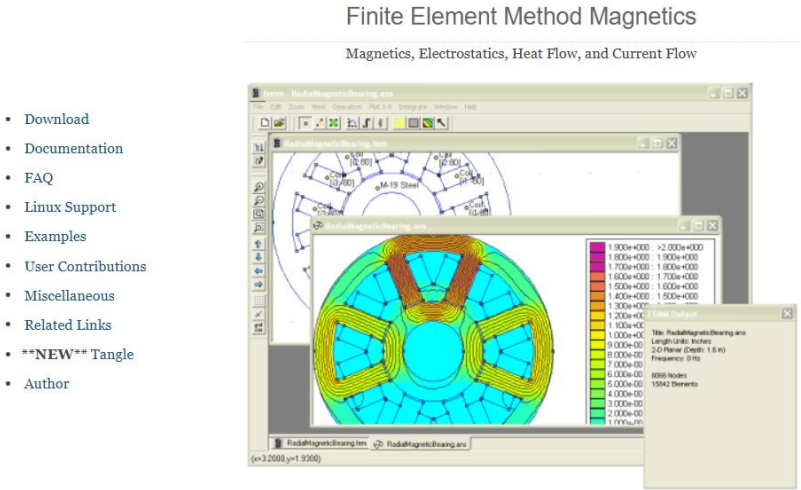
- ▶ Rated current: 55 [A]
- ▶ When 55 [A] is applied through both the top and bottom layers, the current per layer was assumed to be 30 [A] with a design margin.
- ▶ The calculation conditions are as follows:
  - ✓ Ambient temperature: 25 [°C], Temperature rise: 10 [°C], Copper thickness: 3 [oz/ft²]
- ▶ Calculated minimum trace width: 10.9 mm

< Digikey' Trace width caculator >

[*] https://www.digikey.kr/ko/resources/conversion-calculators/conversion-calculator-pcb-trace-width

❖ Actual Temperature Rise of the Trace Width Calculator

- ▶ For a trace width of 10.9 [mm] and a copper thickness of 3 [oz/ft²], the temperature rise was analyzed to verify whether it remains within 10 °C.
- ▶ The analysis was performed using analytical equations and FEMM thermal simulation.
- ▶ FEMM is a free 2D finite element analysis software that supports electromagnetic, heat flow, and current flow analysis.

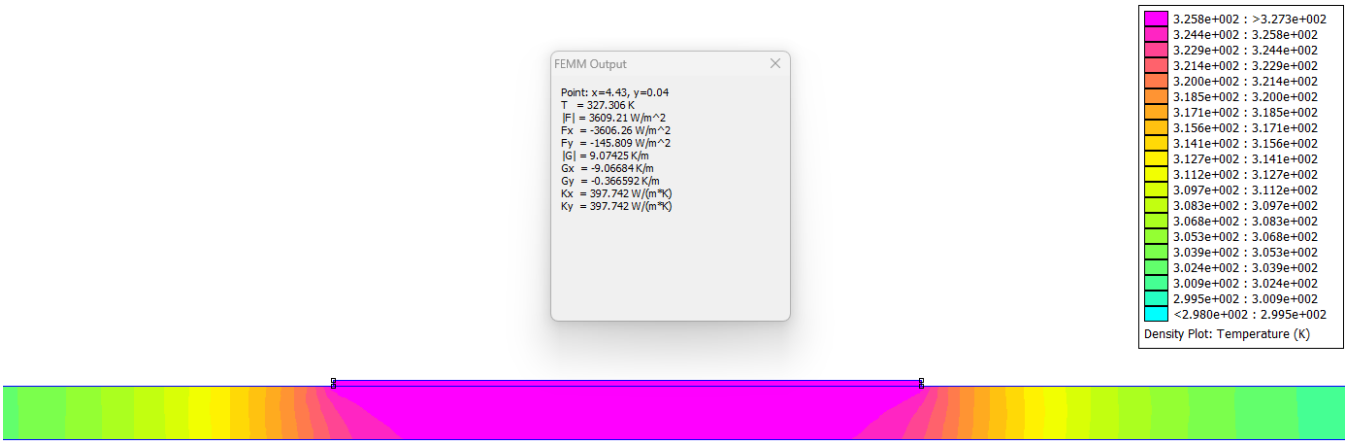


< FEMM Website – Supported Analysis Features >

[*] https://www.femm.info/wiki/HomePage

❖ FEMM Thermal Analysis Result with FR4 Attached Beneath the Trace

- ▶ Trace temperature: 327.306 [K] = 54.306 [°C]
- ▶ Therefore, $\Delta T = 54.306 - 25 = 29.306$ [°C]
- ▶ This temperature rise is significantly lower than the 123.2 [°C] temperature rise obtained when FR4 was not attached.
- ▶ The FR4-based PCB acts as a heat sink.
  - ✓ Due to the thermal conductivity of FR4, the heat from the copper spreads into the PCB and is dissipated.

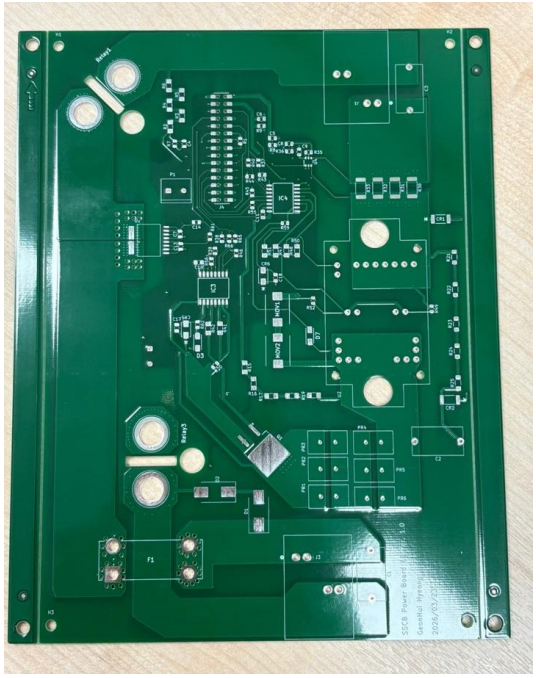


< FEMM Thermal Analysis Result with FR4 Attached Beneath the Trace >

[*] https://www.femm.info/wiki/HomePage

❖ PCB Board & Temperature Test

- ▶ PCB traces were fabricated considering the current level.
- ▶ A thermal camera test will be conducted to verify whether the temperature rise under current flow matches the calculated value.



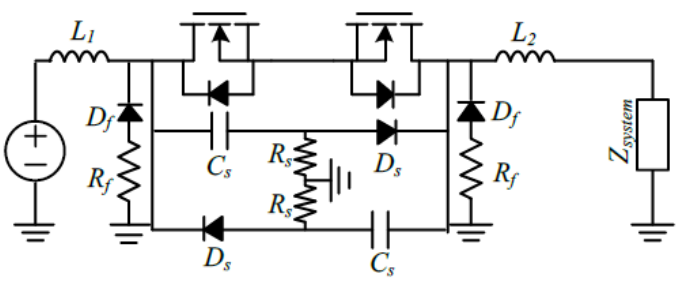
[*] https://www.femm.info/wiki/HomePage

OUTLINE

4 Over Voltage Protection

❖ SSCB Over Voltage

- Since an SSCB interrupts fault current very rapidly, large overvoltage can be generated by the energy stored in the system inductance.
- When the current changes rapidly during interruption, the voltage across the semiconductor switch increases sharply according to $V = L\frac{di}{dt}$
- Since semiconductor devices can fail if their voltage rating is exceeded, overvoltage suppression is essential.
- OVP devices such as snubbers, MOVs, and TVS diodes absorb or dissipate the energy stored in the system inductance to protect the semiconductor device.



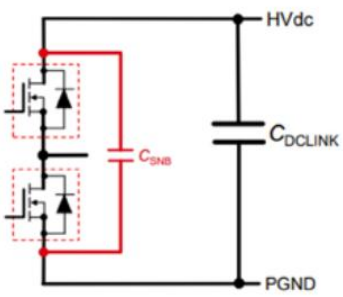
< RCD Snubber Example>

< MOV Example >

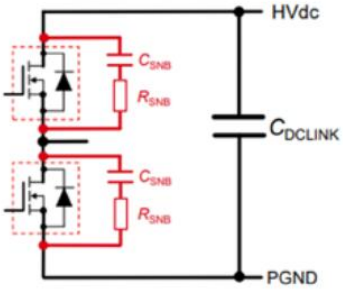
[*] 박동훈. "계통 인덕턴스에 따른 반도체 차단기 과전압 억제 회로 시정수 결정 방법 및 시지연 효과 분석." 국내석사학위논문 서울대학교 대학원, 2019. 서울

❖ Snubber – OVP

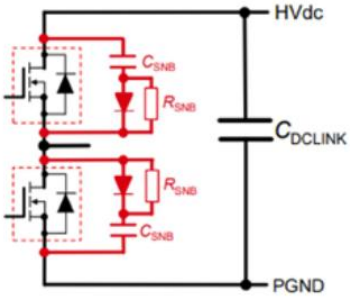
- A C snubber is the simplest snubber that uses only a capacitor to slow the voltage rise across the switch.
- An RC snubber uses a capacitor and resistor to suppress overvoltage and ringing while dissipating the stored energy in the resistor.
- An RCD snubber uses a diode to control the energy-flow direction, stores the energy in a capacitor, and discharges it through a resistor.
- A discharge-suppressing RCD snubber pre-charges the capacitor so that fault-current rise and overvoltage can be suppressed immediately after turn-off.



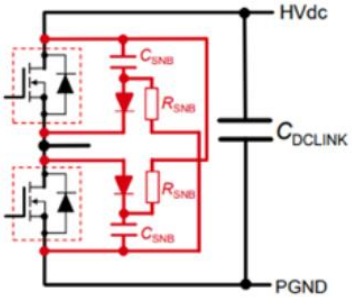
< C Snubber >



< RC Snubber >



< RCD Snubber >

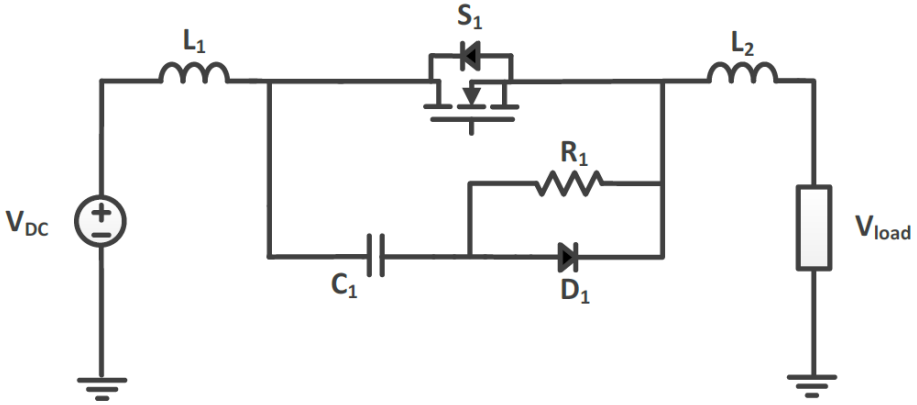


< discharge-suppressing RCD Snubber>

[*] https://techweb.rohm.co.kr/product/power-device/sic/15886/

❖ RCD Snubber

- RCD snubber is referred to as a charge-discharge type RCD snubber.
- A charge-discharge type RCD snubber is composed of a resistor R, capacitor C, and diode D. Its purpose is to suppress the overvoltage generated across the semiconductor switch during fault-current interruption.
- A charge-discharge type RCD snubber can reduce the inrush current during re-closing compared with a simple C snubber.
- However, since the capacitor is not sufficiently charged at the moment of fault occurrence, it cannot immediately suppress the fault current right after turn-off.

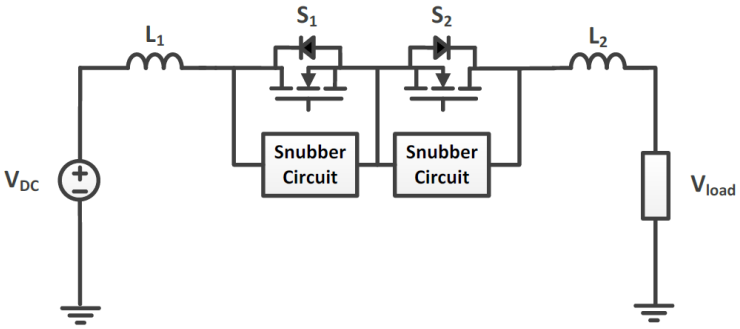


< RCD Snubber >

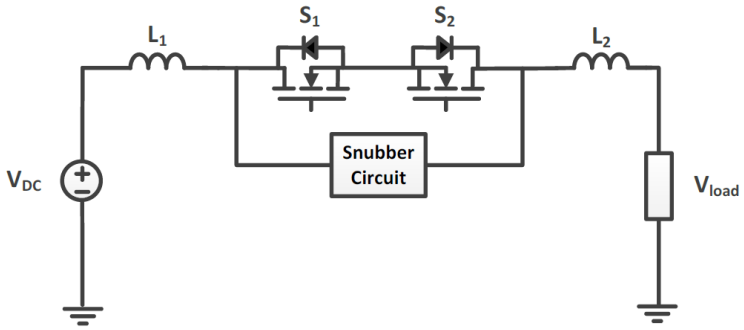
[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Bidirectional SSCB Snubber

- In DC systems, fault current can flow in both directions depending on the fault location, so a bidirectional snubber circuit is required.
- In a bidirectional system, two unidirectional snubber circuits are applied to the two semiconductor switches to handle fault currents in both directions
- In a bidirectional system, one bidirectional snubber circuit is applied across the entire semiconductor breaker to handle fault currents in both directions.



< Bidirectional SSCB using two unidirectional snubber circuits >



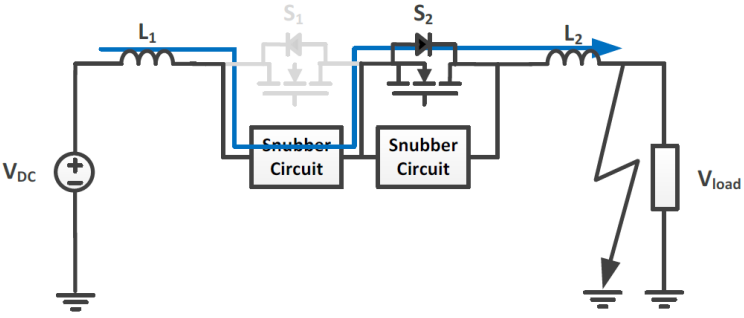
< Bidirectional SSCB using one bidirectional snubber circuit >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

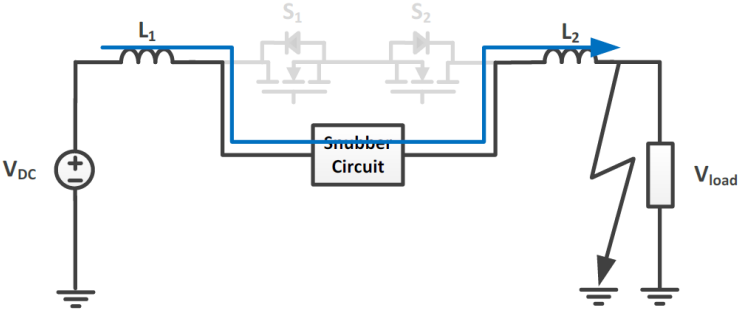
4 Over Voltage Protection

❖ Bidirectional SSCB Snubber

- With two unidirectional snubbers, part of the fault current can flow through the MOSFET body diode.
- This increases conduction loss and thermal stress due to the high forward voltage of the body diode.
- A single bidirectional snubber diverts the fault current into the snubber circuit and protects the semiconductor device.



< Case where the fault current flows
through the body diode during fault-current interruption >

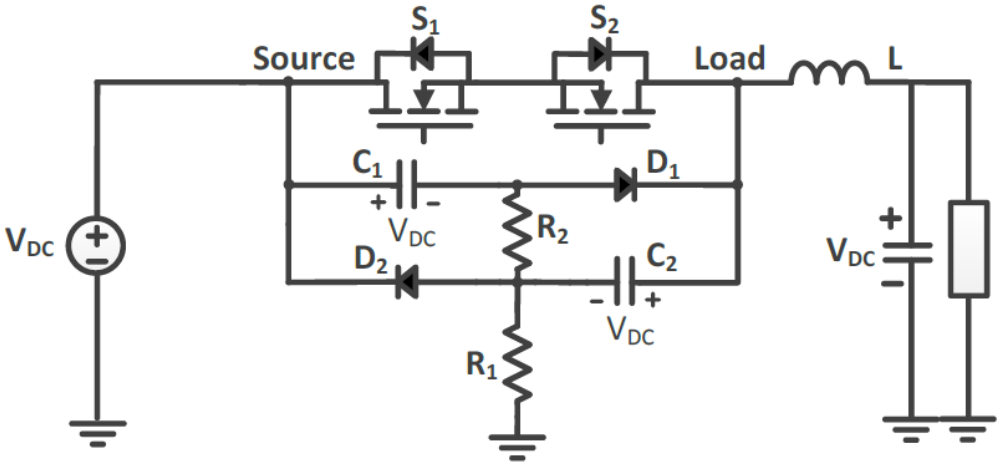


< Case where the entire fault current flows
through the snubber circuit during fault-current interruption >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Bidirectional snubber used in an SSCB

- This structure uses a snubber circuit designed to handle bidirectional fault currents in a DC system.
- The fault current is diverted through the snubber circuit instead of flowing through the body diode of the semiconductor switches, thereby reducing conduction loss and thermal stress in the body diode.
- As a result, the bidirectional semiconductor circuit breaker can improve both overvoltage protection and fault-current suppression performance.

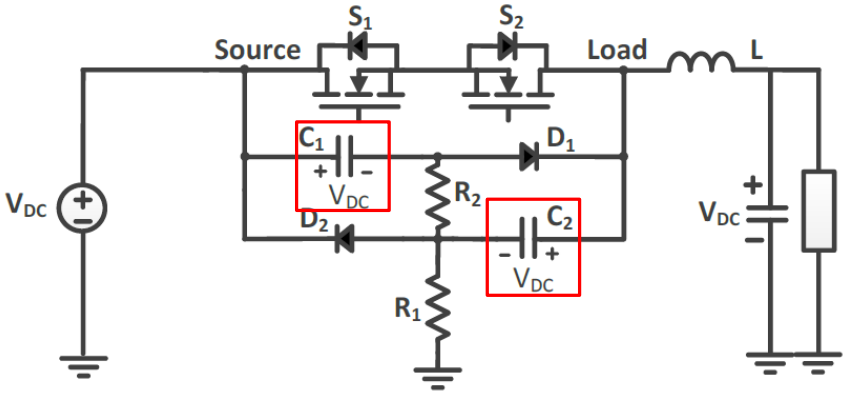


< Bidirectional Snubber Circuit for SSCB >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Snubber Capacitor Selection

- The snubber capacitors C_1 and C_2 absorb the inductive energy during fault-current interruption and limit the semiconductor switch voltage below $V_{max,sw}$.
- Design Equation :
  - ✓ $C \geq L\left(\frac{I_{fault}}{V_{max,sw} - V_{DC}}\right)^2$
    - L : Equivalent inductance to be handled by the snubber
    - I_{fault} : Fault current at the moment of semiconductor turn-off
    - $V_{max,sw}$: Maximum allowable switch voltage

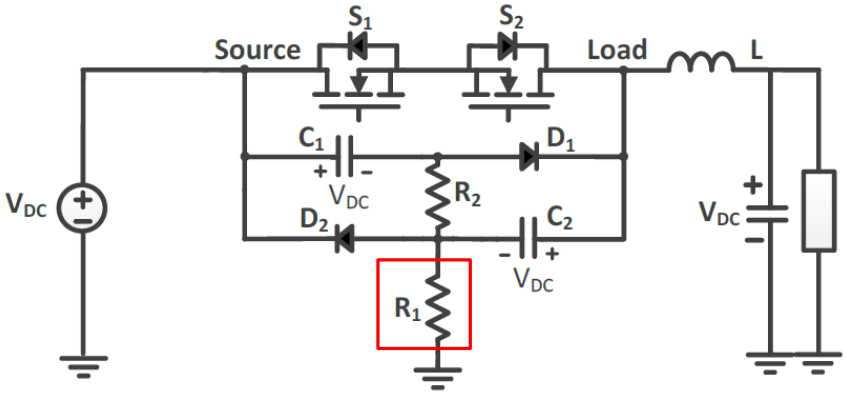


< Bidirectional Snubber Circuit for SSCB >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Snubber R_1 Selection

- R1 determines the additional current flowing through the snubber during a source-side short-circuit fault.
- A smaller R_1 can improve fault detection and current suppression, but it increases the instantaneous current stress of the semiconductor switch.
- Design Equation :
  - ✓ $R_1 \geq \frac{V_{DC}}{I_{max,sw} - I_{rated}}$
    - I_{rated} : Rated current under normal operation
    - $I_{max.sw}$: Maximum current capability of the semiconductor switch

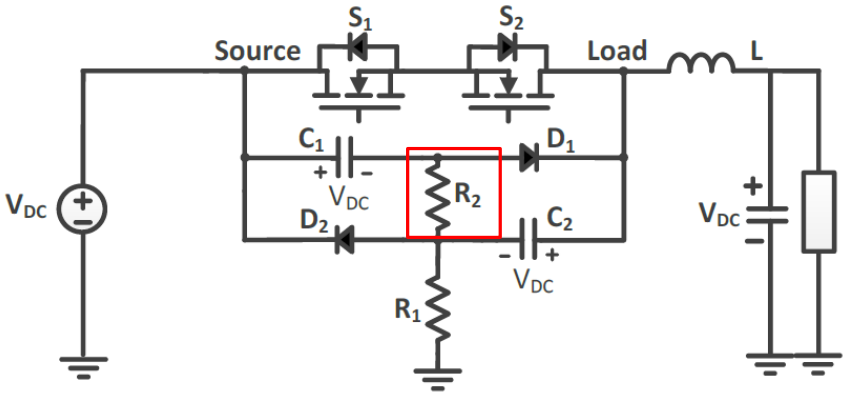


< Bidirectional Snubber Circuit for SSCB >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Snubber R_2 Selection

- R2 determines the initial output voltage of the snubber circuit immediately after turn-off.
- In a load-side short-circuit fault, the fault current rises up to the protection level before interruption; therefore, a low initial snubber voltage can increase the fault-current peak.
  - ✓ $R_2 \geq \frac{R_1 V_{DC}}{R_1 I_{fault} - V_{DC}}$

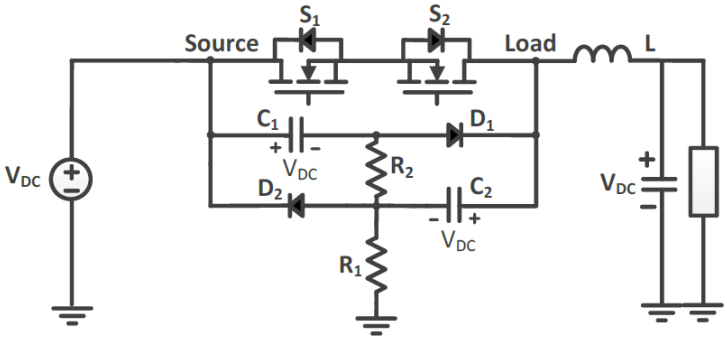


< Bidirectional Snubber Circuit for SSCB >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ Design Equation-Based Component Selection

- ▶ Component values are selected based on the preceding design equations.
  - ✓ $C \geq L\left(\frac{I_{fault}}{V_{max,sw}-V_{DC}}\right)^2 = 20[\mu F](\frac{250[A]}{1400[V]-1000[V]}) = 7.8125[\mu F] \approx 8[\mu F]$
  - ✓ $R_1 \geq \frac{V_{DC}}{I_{max,sw}-I_{rated}} = \frac{1000[V]}{525[A]-350[A]} = 5.714[\Omega]$
  - ✓ $R_2 \geq \frac{R_1 V_{DC}}{R_1 I_{fault}-V_{DC}} = \frac{5.714[\Omega]\times 1000[V]}{525[A]-350[A]} = 13.33[\Omega]$
- ▶ These can be increased to limit snubber discharge current, reduce current stress, and adjust the over voltage.
- ▶ The final component values can be modified.

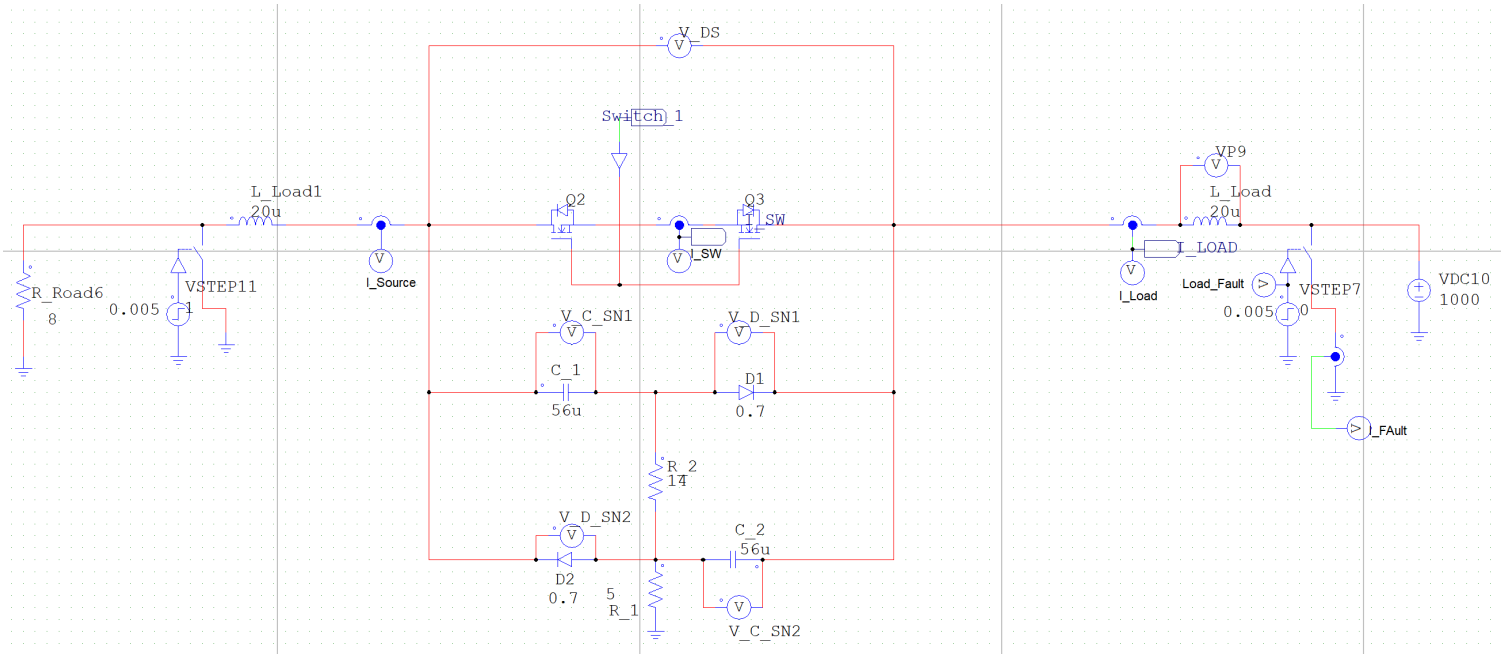


< Bidirectional Snubber Circuit for SSCB >

[*] 신동호. "SiC MOSFET을 사용한 DC 반도체 차단기의 비대칭 스너버 회로 연구." 국내석사학위논문 서울대학교 대학원, 2018. 서울

❖ OVP Snubber simulation circuit

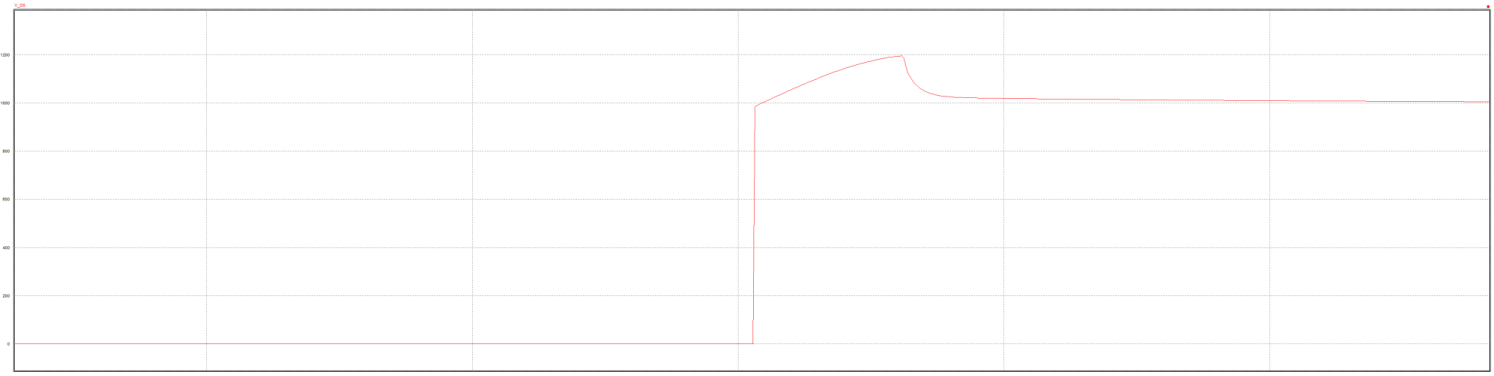
- ▶ The figure below shows the snubber circuit implemented in PSIM.
- ▶ The circuit includes switches used to simulate short-circuit faults.
- ▶ The component values selected using the previous design equations were adjusted through multiple simulations.



4 Over Voltage Protection

❖ OVP Snubber simulation Result

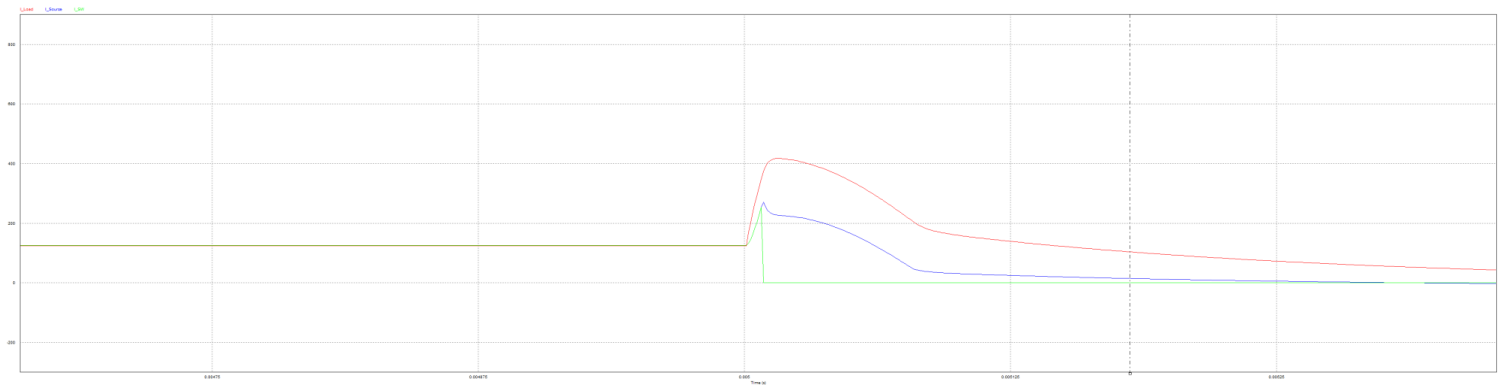
- ▶ This waveform shows the interruption behavior of the semiconductor circuit breaker and snubber circuit after a load-side short-circuit fault occurs.
- ▶ The peak voltage across the semiconductor switch, V_{DS} ,is **1195.4 [V]**, which is successfully limited below the maximum voltage limit of **1400 [V]**.



4 Over Voltage Protection

❖ OVP Snubber simulation Result

- ▶ In the lower waveform, the green trace represents the semiconductor device current, which rapidly decreases to 0 A after fault detection.
- ▶ This indicates that the semiconductor switch is successfully turned off.
- ▶ The red trace represents the load current, and the blue trace represents the source current.
- ▶ After the switch is turned off, both currents do not disappear immediately but gradually decay.



❖ SSCB Non-Linear Over Voltage Protection

- SSCB Non-Linear Over Voltage Protection is a protection method that limits the overvoltage generated during semiconductor interruption using non-linear devices such as MOVs or TVS diodes.
- MOVs or TVS devices conduct only when the switch voltage exceeds a certain level, diverting the fault energy into another path and clamping the V_{DS} peak.
- Non-linear OVP works as a final voltage clamp to suppress transient overvoltage that cannot be fully handled by the snubber circuit alone, protecting the semiconductor devices in the SSCB.

< TVS Diode Example >

< MOV Example >

OUTLINE

❖ SSCB Solid-state device

- The solid-state device in an SSCB is the main semiconductor switch that interrupts current without mechanical contacts.
- It enables fault-current interruption within tens of microseconds, but it must withstand high voltage stress
- High transient current because system inductance generates overvoltage during turn-off.
- Various power semiconductor devices can be used in SSCBs, such as IGBT, SiC MOSFET, SiC JFET.

< infineon's cool SiC MOSFET >

[*] Gate Driver Finder | Infineon Technologies

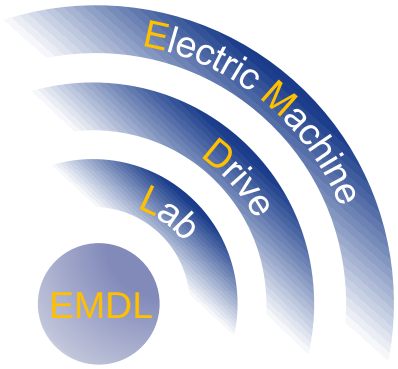
❖ SSCB Solid-state device comparison

	IGBT	SiC MOSFET	SiC JFET
Voltage / Current	Suitable for high-voltage and current applications	Suitable for high-voltage and speed switching	Suitable for high-voltage, low-resistance, and fast interruption
Switching Speed	Relatively slow	Fast	Fast
Turn-off Characteristic	Has tail current	Almost no tail current	Capable of fast interruption
Conduction Loss	Can be advantageous at high current	Low $R_{DS(on)}$	Very low $R_{DS(on)}$ is possible
SSCB Suitability	Applicable, but less advantageous in terms of loss and speed	Suitable for SSCBs	Highly suitable for SSCBs, but normally-on behavior must be considered

< infineon's cool SiC JFET >

[*] https://www.infineon.com/product-information/power/silicon-carbide-jfets

Thank you



Performance Improvement of a Two-Stage Classification Algorithm in a Cloud-Based MCI Screening System

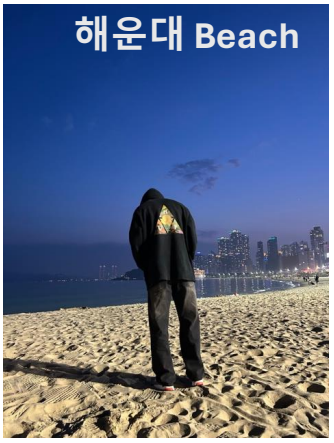
Nagoya Institute of Technology
M1　Sogo Ohtsu

Contents

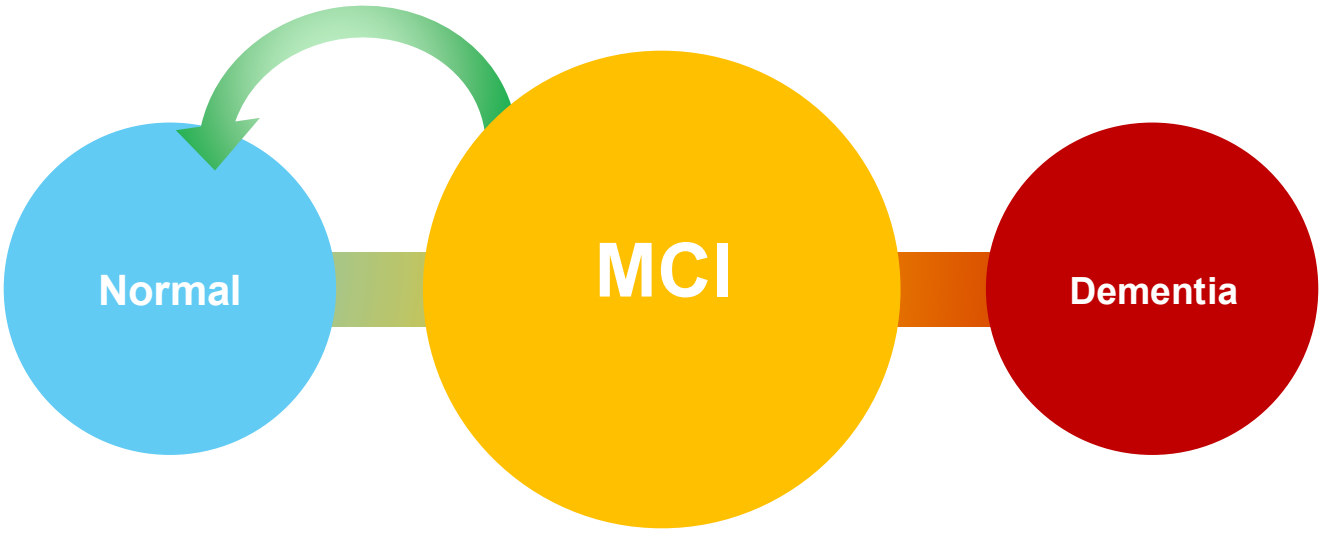
0. Trip in Korea

소울

푸산



1. Backgrounds 1



Mild Cognitive Impairment（**MCI**）
The stage where mild cognitive impairment is recognized

Appropriate interventions can revert MCI to Normal

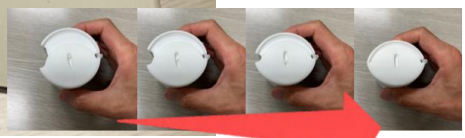
Detecting MCI by Using iWakka

What is iWakka?

Tohu (두부)

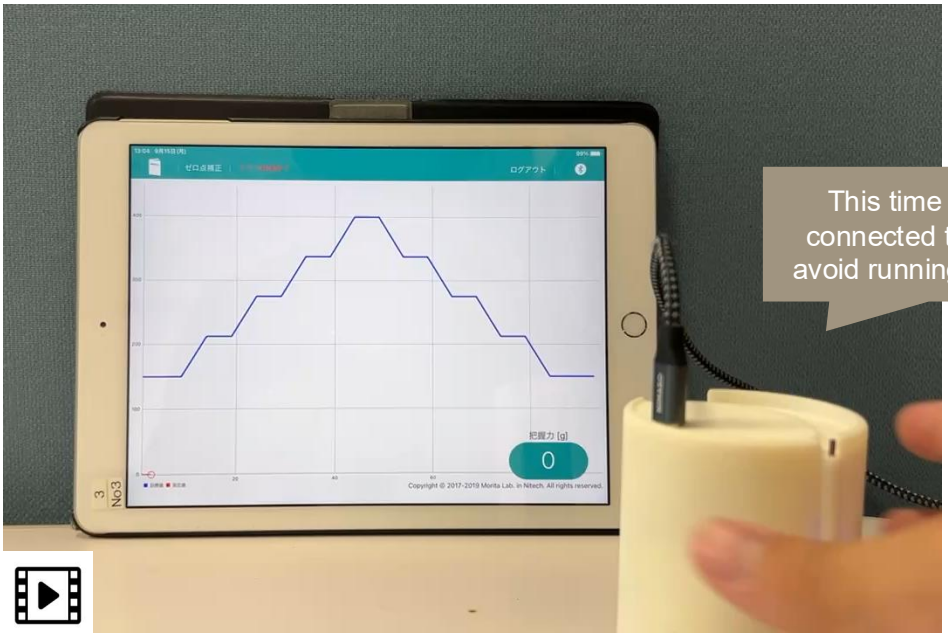
A device for measuring the grasping force of the user when grasping a soft material

Can be charged and **wireless**



0g (min) grasping force 400g (MAX)

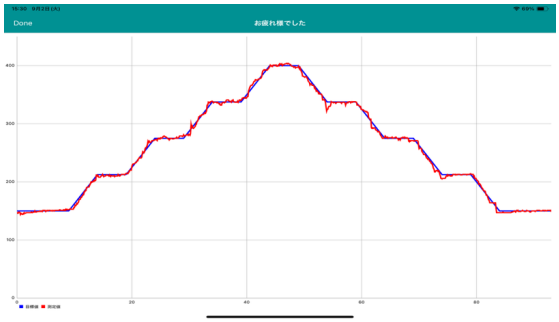
How to Use



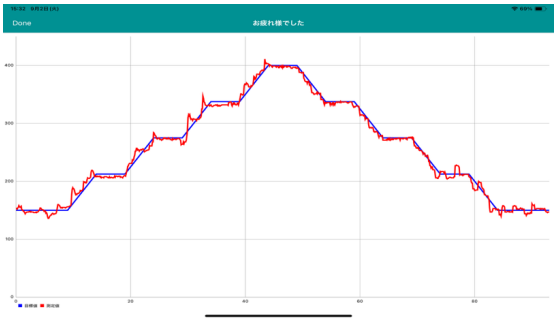
This time iWakka was connected to the cable to avoid running out of battery

- Red point moves vertically according to the user's grasping force
- Users try to adjust their grasping force to keep the red point along the blue line

How to Evaluate



$AGFscore$ is low
（Superior grasping control ability）



$AGFscore$ is high
（ Inferior grasping control ability ）

- AGF : Adjustability for Grasping Force
  The ability to modulate grasping force through muscle contraction control
- Learning Rate （LR）

$$AGFscore\ [\mathrm{g}] = \frac{1}{N}\sum_{k=1}^{N}|f(k) - f_d(k)|$$

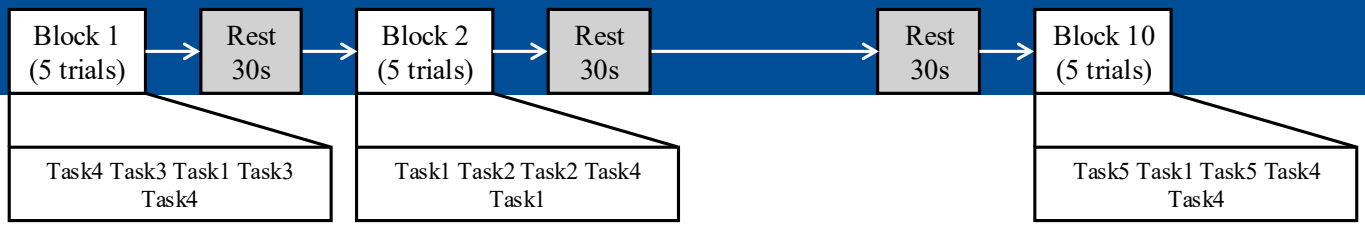
$f(k)$: Measured Force[g]
$f_d(k)$: Target Force[g]
N: Number of samples in the evaluation period

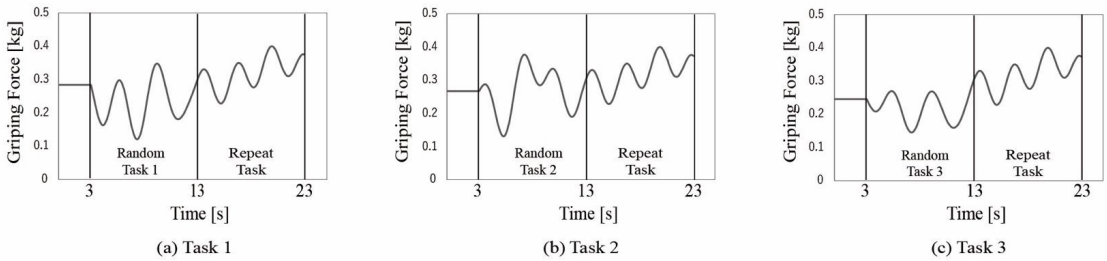
$$LR^j = \frac{\overline{AGF}^1 - \overline{AGF}^j}{\overline{AGF}^j}$$

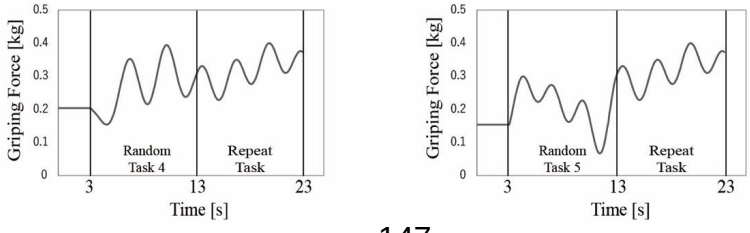
$\overline{AGF}^j$: AGF in Block j

Subjects：126 elderly individuals
Tasks： 5 kinds of waveforms combined from two sine waves（23seconds × 5trilas × 10blocks

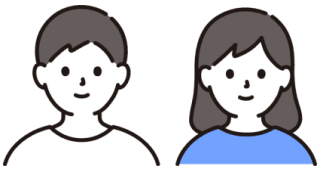
Protocol

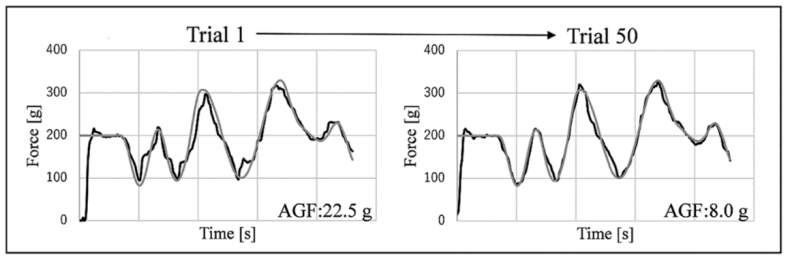






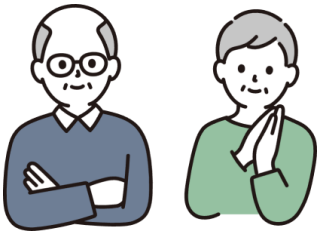
Young Adults（YA）

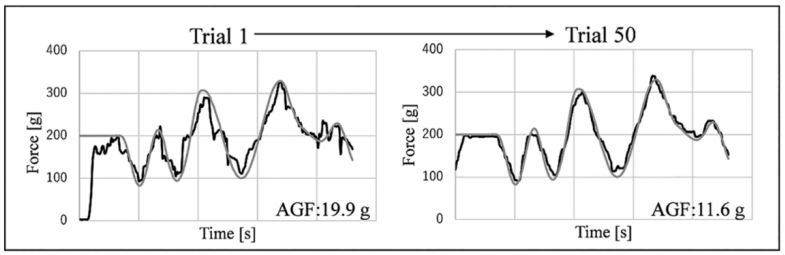




(A) Subject in the YA group

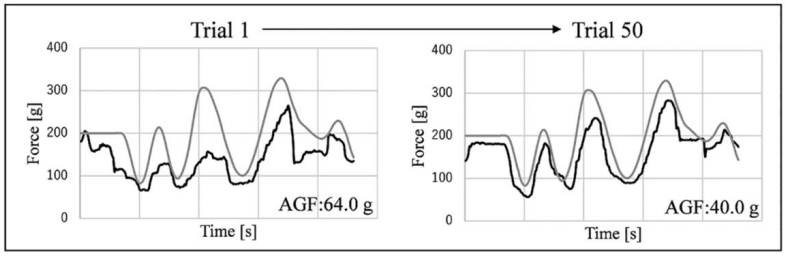
Older Adults（OA）



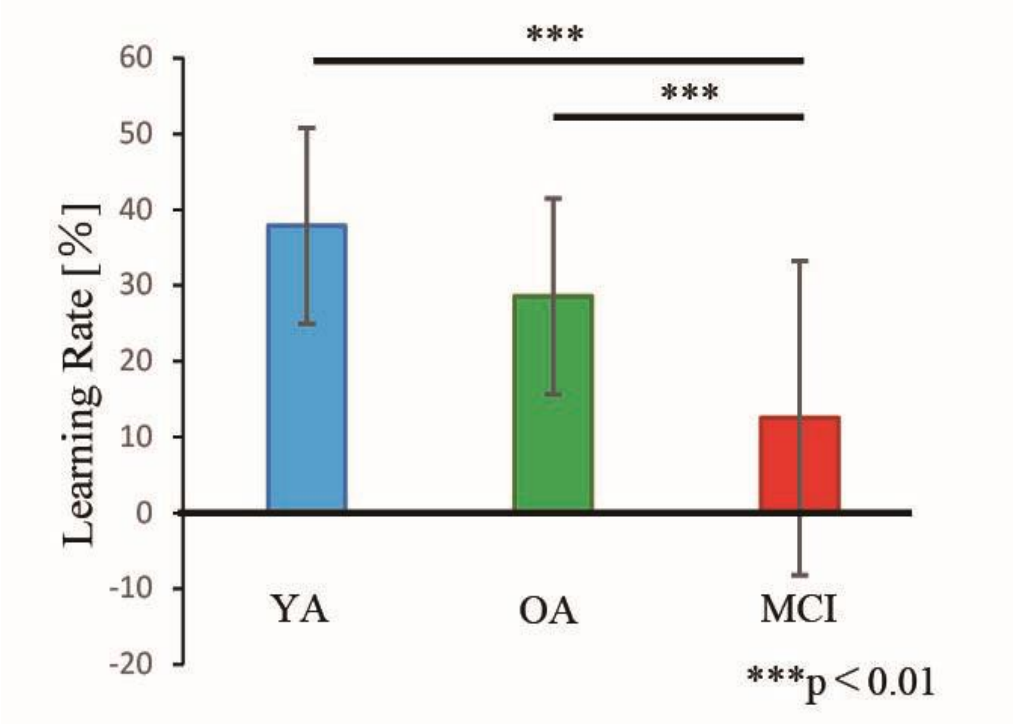


(B) Subject in the OA group

MCI



(C) Subject in the MCI group



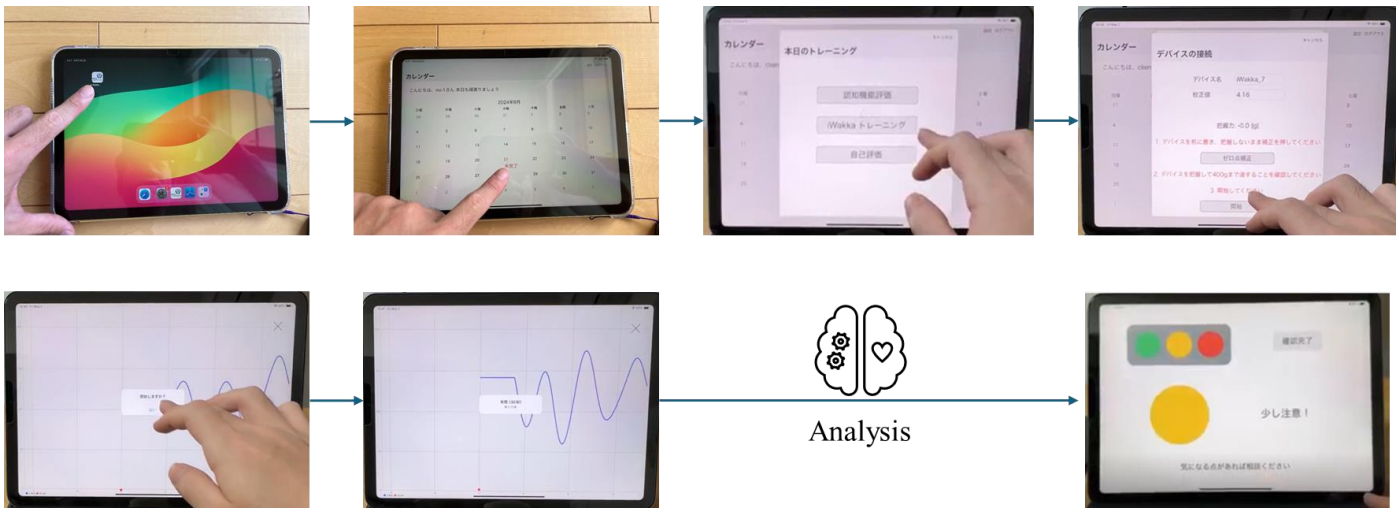
n=28 n=27 n=11

Detect significant differences between YA and MCI, OA and MCI

➡ **Learning Rate** is an effective variance to classify users to Normal or MCI

1. Backgrounds 8

iWakka Health Care System

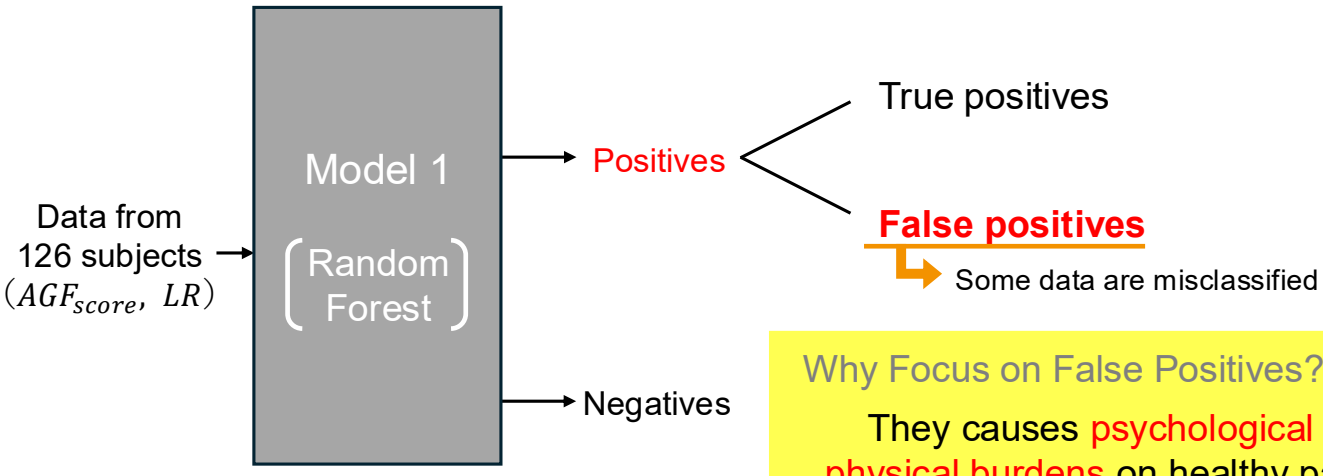


Result:
Green（Normal）
Yellow（Mild Impairment）
Red（Severe Impairment）

Evaluate user's cognitive skills in 15 minutes

2. Experimental Methods 9

Toshima (2025)：Created MCI screening model
Area Under the Curve（AUC）：0.81

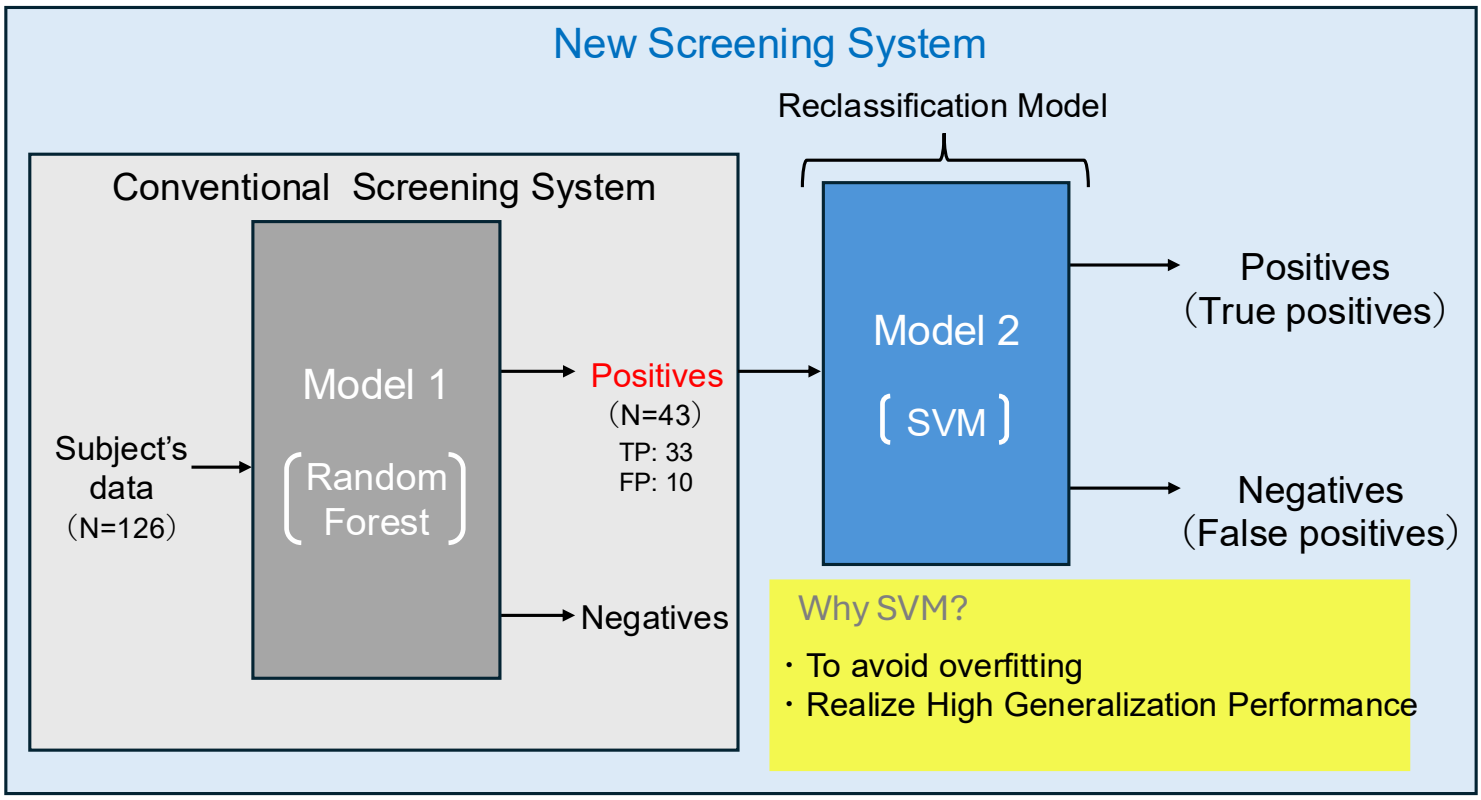


Why Focus on False Positives?

They causes psychological and physical burdens on healthy patients
➡ Hinders the optimal allocation of medical resources

→Address this problem by re-classifying positives into True Positives or False Positives

Reducing false positives by applying two-stage model and improve the performance of the MCI screening system



Constructing procedure of reclassification model

"False positives exhibit inconsistent motivation"

Focus on AGF variance

Calculate 5 kinds of variables can reflect AGF variance

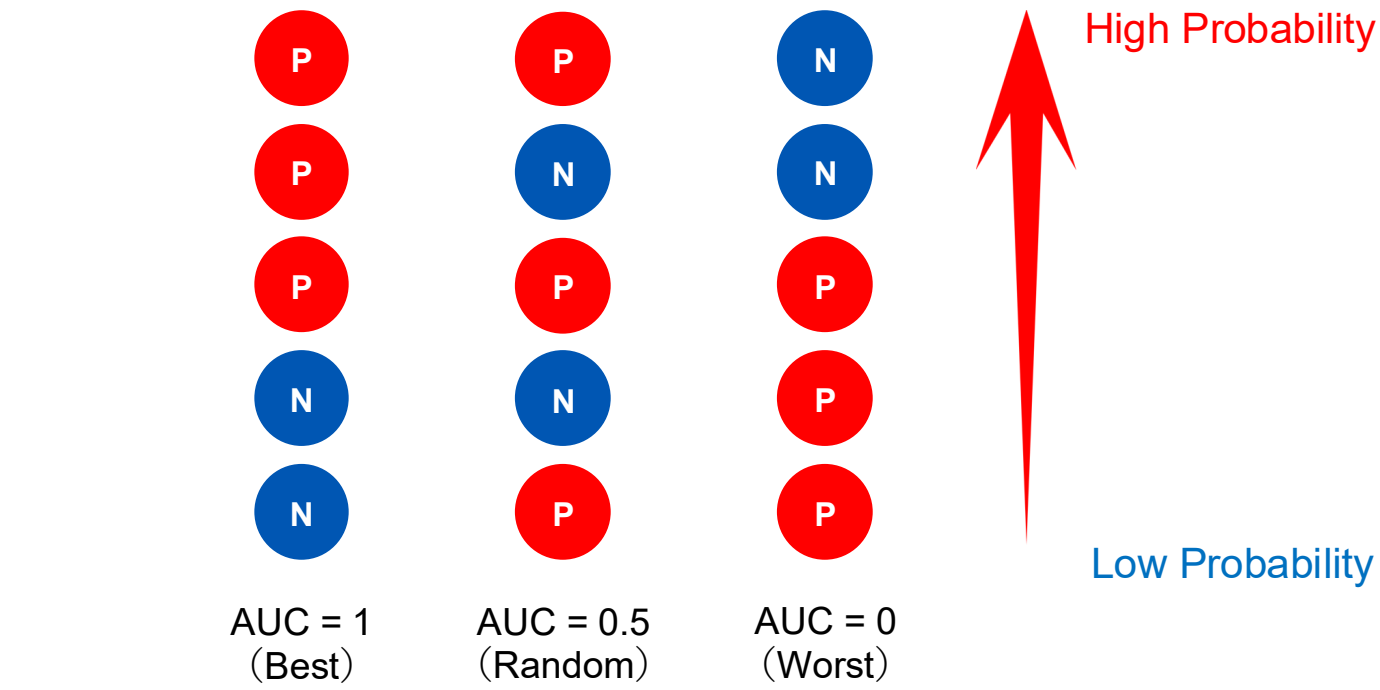
Use Support Vector Machine（SVM）

Model performance was evaluated by calculating the AUC using 5-fold stratified cross-validation.

AUC

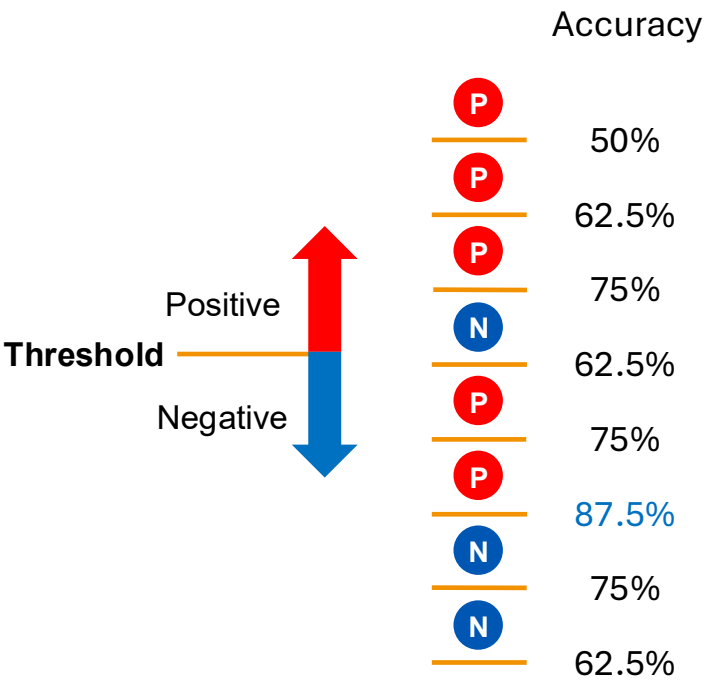
→The ability to rank subjects by their probability of being positive（MCI）

Example) 5 Subjects（3 Positives, 2 Negatives）

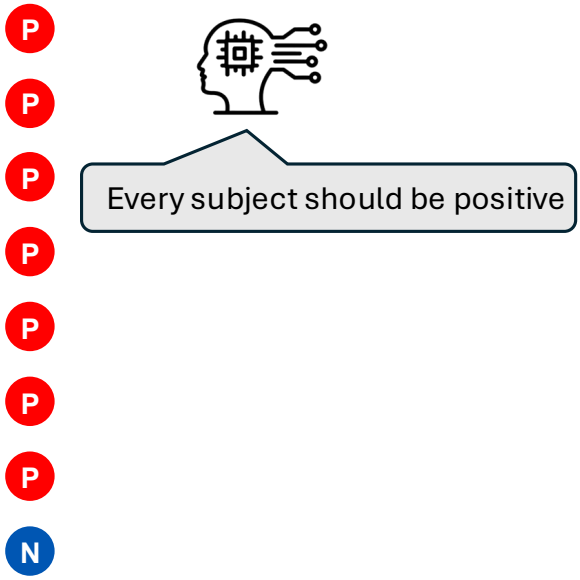


Why not Accuracy?

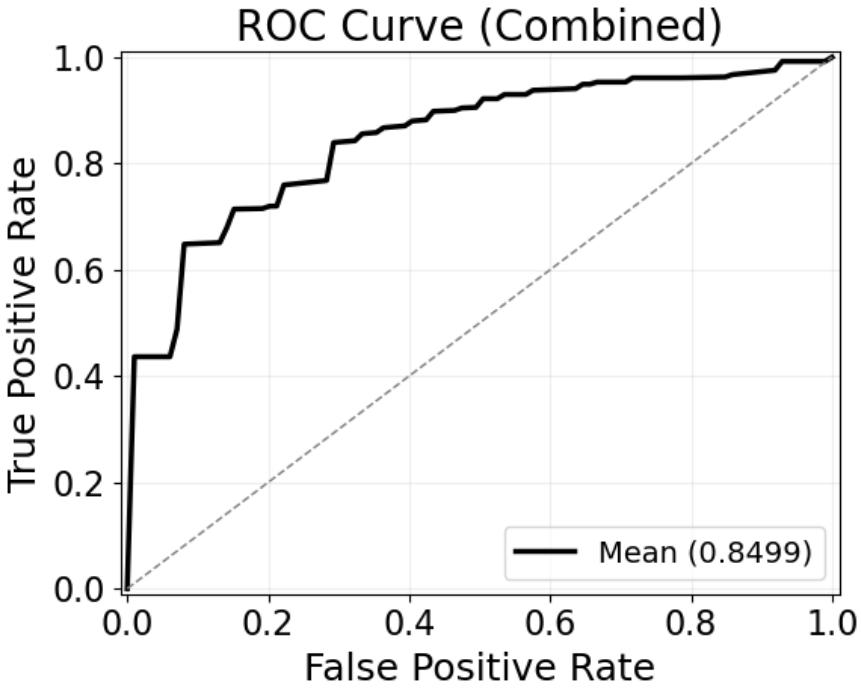
① Threshold Dependency



② Imbalance Sensitivity



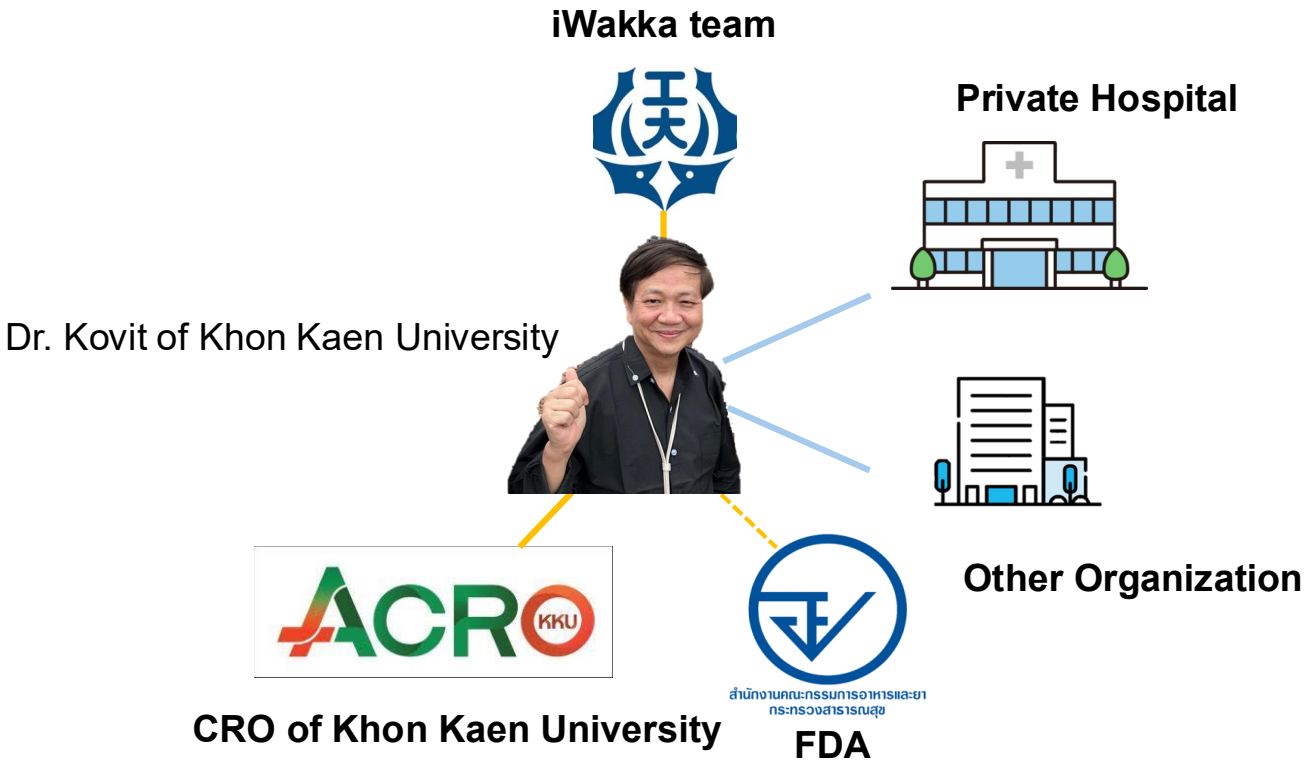
Combined Model AUC



Combined Model AUC : **0.85** （Conventional Method : 0.81）

→Contribute to Reducing False Positives

Collaborative Research is in the Works



Objective

Reducing false positives by applying two-stage model and improve the performance of the MCI screening system

Results

Improved AUC to 0.85

➡ Enabled more precise classification of the borderline between positive and negative cases than conventional methods

Future Works

- Redefining features
- Incorporating ongoing data in Tobishima city


Thank you for your attention
My hometown, Kyoto City from Mt. Daimonji

High-Efficiency Isolated Single-Phase Inverter Using a Phase-Shifted Full-Bridge Converter and Unfolding circuit With DQ-Repetitive Control

PEEC Laboratry

2026 Joint University Student Workshop

2026. 05. 14

Presenter : Eun Seop Kim

Author : Eun Seop Kim, Su Ho Park, Hag Wone Kim†

E-mail : kls4010@a.ut.ac.kr

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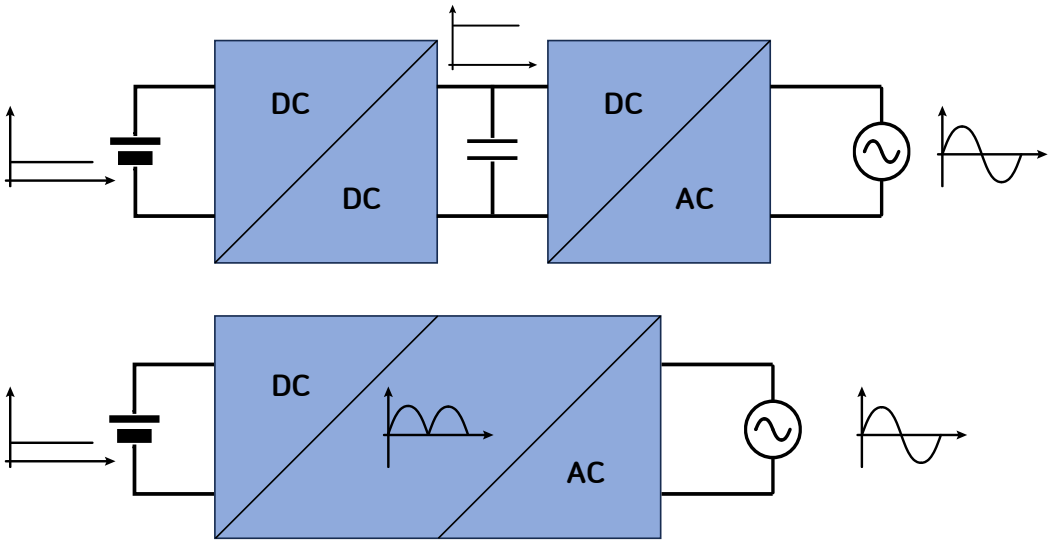
PEEC Laboratry

System Architecture of the Unfolding Circuit

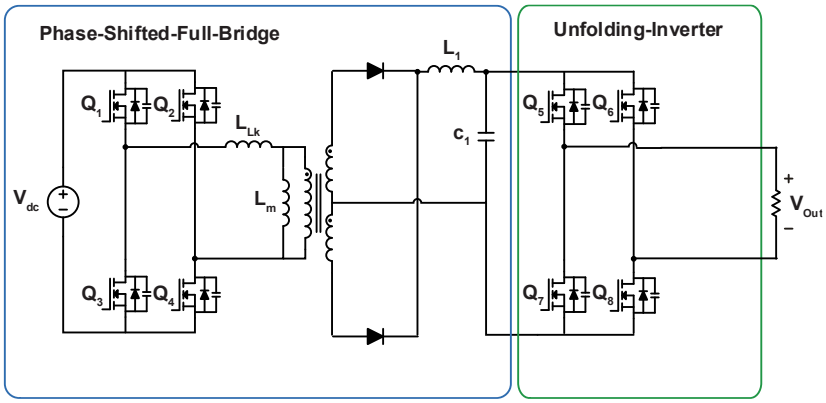
▪ System Architecture of the Unfolding Circuit

▪ Operation of the Unfolding Circuit

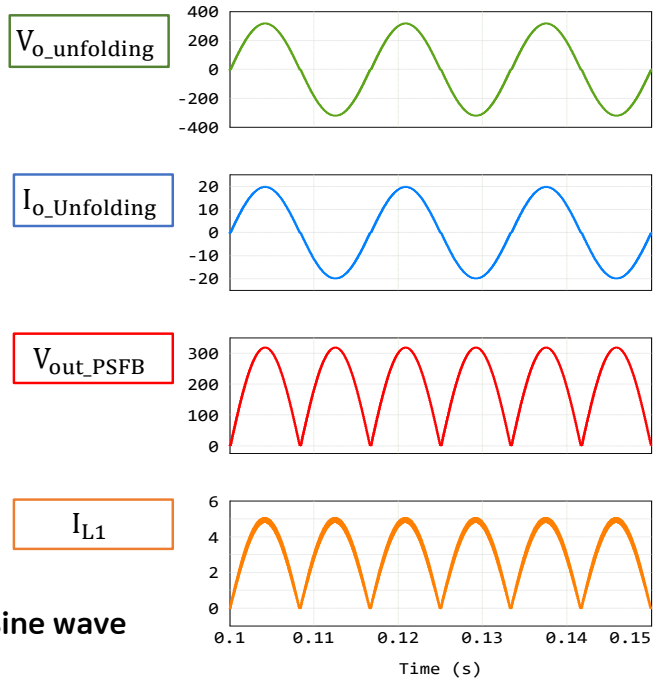


- Unlike conventional PWM inverters, the unfolding circuit operates in a single stage where the DC/DC converter generates the absolute value of a sine wave, and the DC/AC inverter performs polarity reversal control.

▪ PSFB-Unfolding Inverter Open Loop



<PSFB-Unfolding Inverter>



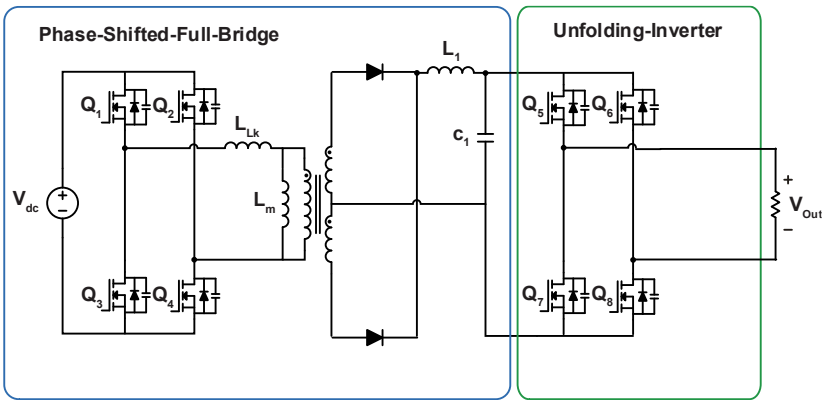
▪ The unfolding circuit inverts the absolute value of the sine wave to generate a pure sine wave.

Analysis of Output Voltage Waveform Distortion Causes

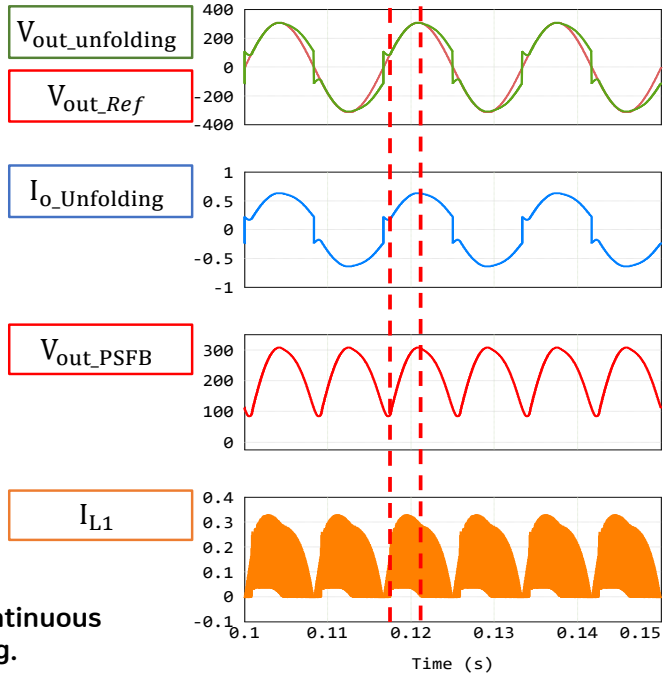
▪ Analysis of Output Voltage Waveform Distortion Causes

PEEC Laboratry

▪ Main Waveform Under Light Load Conditions



<PSFB-Unfolding Inverter>

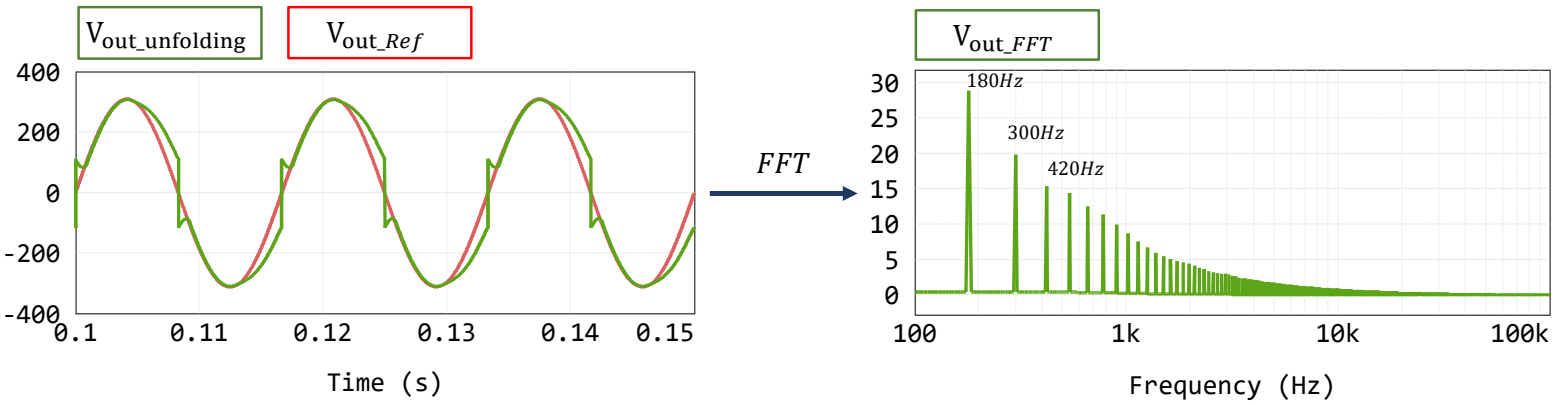


- Under light load conditions, the L1 current enters DCM (Discontinuous Conduction Mode), preventing the C1 voltage from discharging.

▪ Analysis of Output Voltage Waveform Distortion Causes

PEEC Laboratry

▪ Output Voltage FFT Analysis



- It is confirmed that odd harmonic components appear in the output voltage FFT results.
- As the light load condition becomes more severe, the gain values of the odd harmonic components increase.
- Control is required for both the CCM region and the DCM region.

Distortion Reduction Methods or Control Strategies

▪ Reference Paper 1

2488 IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 69, NO. 3, MARCH 2022

Feasibility Study of Model Predictive Control for Grid-Connected Twisted Buck–Boost Inverter

Oleksandr Matiushkin, *Graduate Student Member, IEEE*, Oleksandr Husev, *Senior Member, IEEE*, Jose Rodriguez, *Life Fellow, IEEE*, Hector Young, *Member, IEEE*, and Indrek Roasto, *Member, IEEE*

***Abstract*—This article studies the model predictive control (MPC) for a twisted buck–boost inverter based on unfolding circuit. The focus is on the practical implementation of the MPC algorithm for the microcontroller designed for application in power electronics. Selection of proper cost function parameters along with a continuous control set reduced prediction horizon, at the same time keeping good quality of the grid current. The results showed that simplified differential equations and a multicore microcontroller contribute to the sample time reduction, which in turn increases the sampling frequency with the corresponding increase in the output current quality. The simulation and experimental results confirmed theoretical predictions. In conclusion, the MPC technique suits for reducing zero-crossing distortion and in applications based on unfolding circuit.**

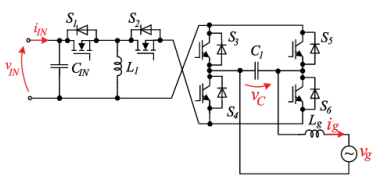
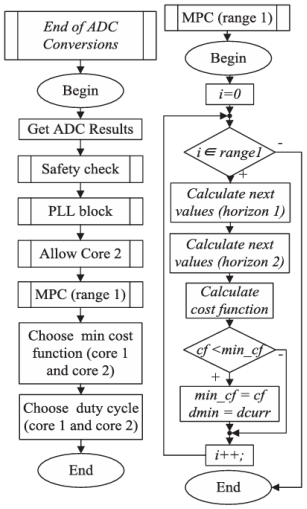


Fig. 1. Buck–boost twisted dc–ac converter based on unfolding circuit.



< MPC algorithm >

- Because the complex calculation process takes place inside the MCU(Model Predictive Control), a high-performance MCU must be used.
- Compared to the basic control method, there are drawbacks in that the number of sensors increases and the model accuracy is sensitive.

- Reference Paper 2

Precise tracking of highly nonlinear phase-shift full-bridge series resonant inverter via iterative learning control

Minsung Kim

Division of Electronics and Electrical Engineering, Dongguk University, Seoul, 04620, Republic of Korea

ARTICLE INFO

Keywords:
Nonlinear dynamics
Wide operating range
Grid voltage disturbance
Iterative learning controller
First harmonic approximation
Global convergence

ABSTRACT

This paper presents iterative learning control of the phase-shift full-bridge series-resonant inverter (PSFB-SRI). It has the merits of high conversion efficiency, medium-to-high power capacity, compact size, and low current–voltage stress on components, but the demerits of highly nonlinear dynamics that varies in a wide range depending on the operating points. The PSFB-SRI also suffers from a grid-voltage disturbance when it operates in grid-connected environment. To overcome these control problems, an iterative learning controller (ILC) supplemented with a proportional controller is developed and applied to the PSFB-SRI. Conventional proportional controller is used to improve the output current tracking performance. The ILC makes use of both previous-cycle and current-cycle learning terms which help the system output to converge to the reference trajectory. It is also simple in structure and easy to implement in practical applications. First-harmonic approximation of the PSFB-SRI model has been conducted and the resulting nonlinear large-signal model was used to construct the developed ILC. A detailed design guideline of the control parameters is provided. Numerical simulations validate the proposed control scheme, and experiments using a 500-W prototype demonstrate its feasibility.

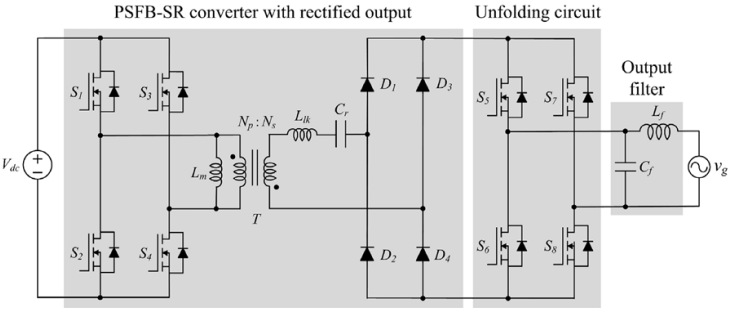
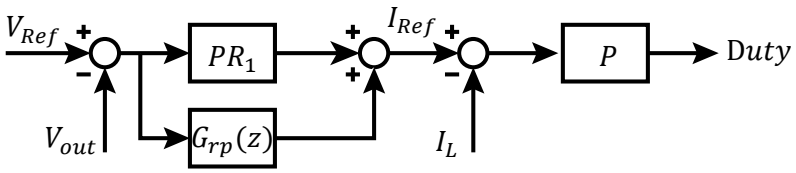


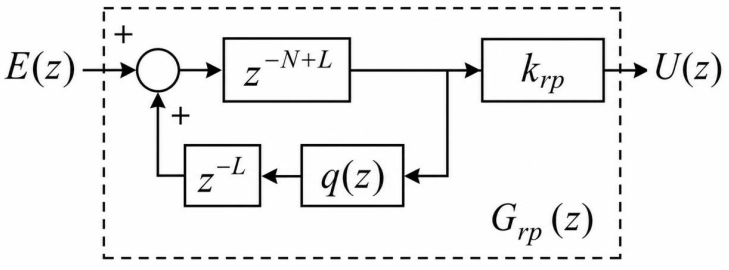
Fig. 1. Circuit diagram of the PSFB-SRI. Components and processes are described in the text.

- This paper uses ILC (Iterative Learning Control), a nonlinear controller, which requires complex calculations to be performed within the MCU.
- A typical unfolding inverter uses complex control to reduce THD.

- Proposed Control Method



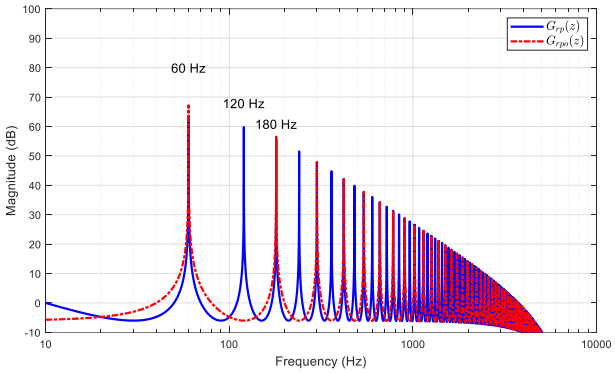
< Proposed Block Diagram >



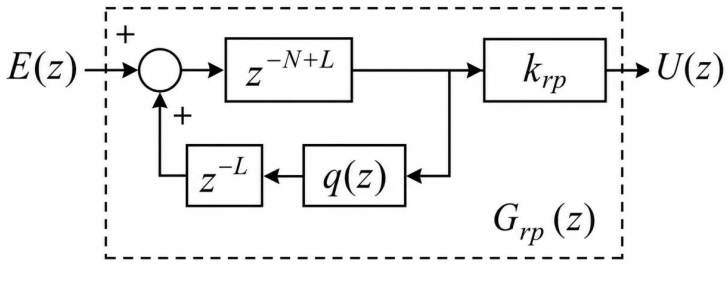
< Block Diagram of Grp(z) >

- PR control is used to directly regulate the AC voltage.
- A repetitive controller is used in parallel to compensate for the gain values of harmonic components.
- P control is used as the current controller.

▪ Characteristics of the Repetitive Controller



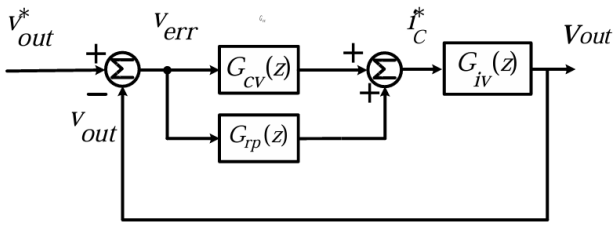
<Bode Plot of the Repetitive Controller >



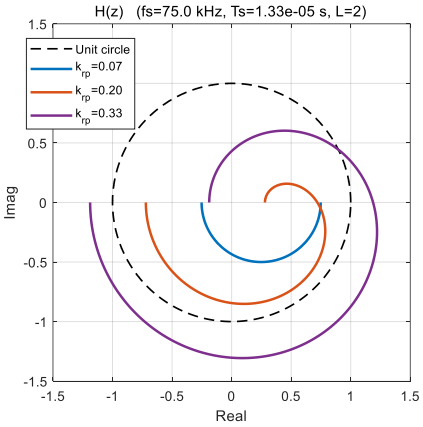
< Block Diagram of Grp(z) >

- The repetitive controller is a method that generates an error model and adds it to the existing controller.
- Repetitive errors are stored in digital memory and output over time during the controller computation process.

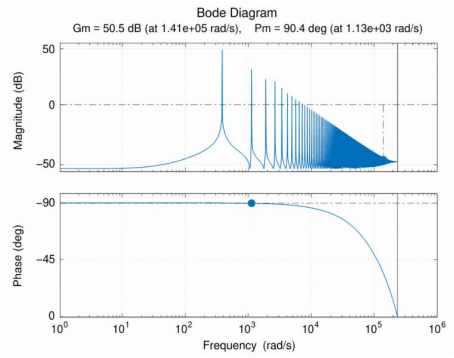
▪ Krp Gain Selection Method



< Parallel Structure of Voltage PR and Repetitive Controller >



<Overall System Stability Evaluation>



<Bode Plot of the Configured Repetitive Controller>

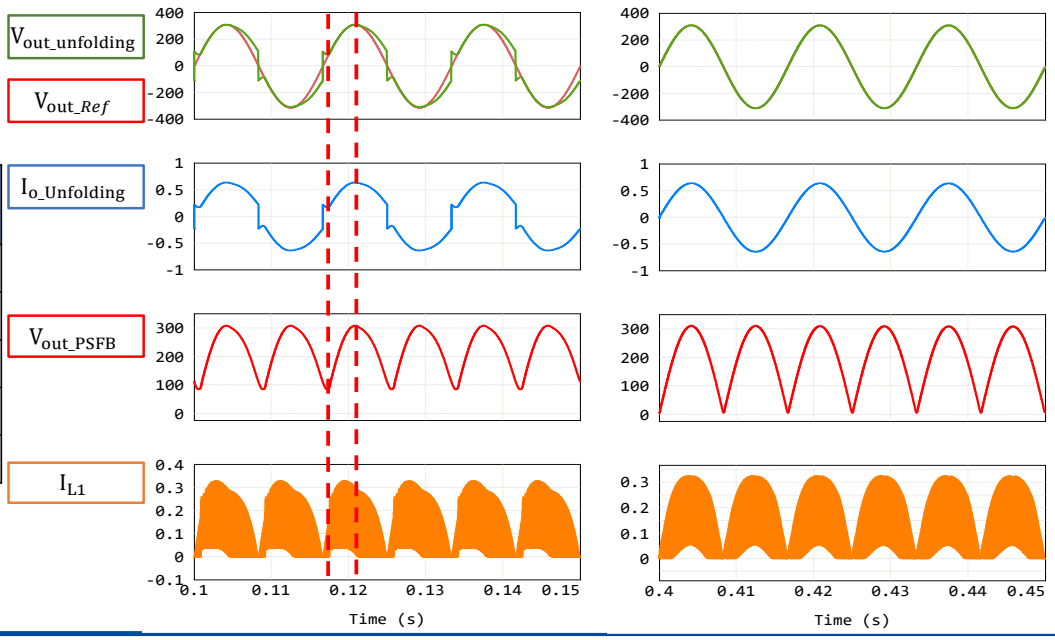
- $G_e(z) = \frac{V_{out}}{V_{out}^*} = \frac{\left(G_{cv}(z)+G_{rp}(z)\right)G_{iv}(z)}{1+\left(G_{cv}(z)+G_{rp}(z)\right)G_{iv}(z)}$
- $G_{rp}(z) = K_{rp} * \frac{-z^{-L}}{\frac{N}{z^2}+q(z)}$
  - $\left(L = 2,\ q(z) = \frac{z+2+z^{-1}}{4},\ N = 1250\right)$
- $G_{cv}(z) = \frac{0.00066z^2-0.00066}{z^2-2z+0.9997}, G_{iv} = 0.036$

- Stability requires all poles to be located inside the unit circle.
- L, N, and q(z) are generalized in the repetitive controller.

▪ Simulation Results

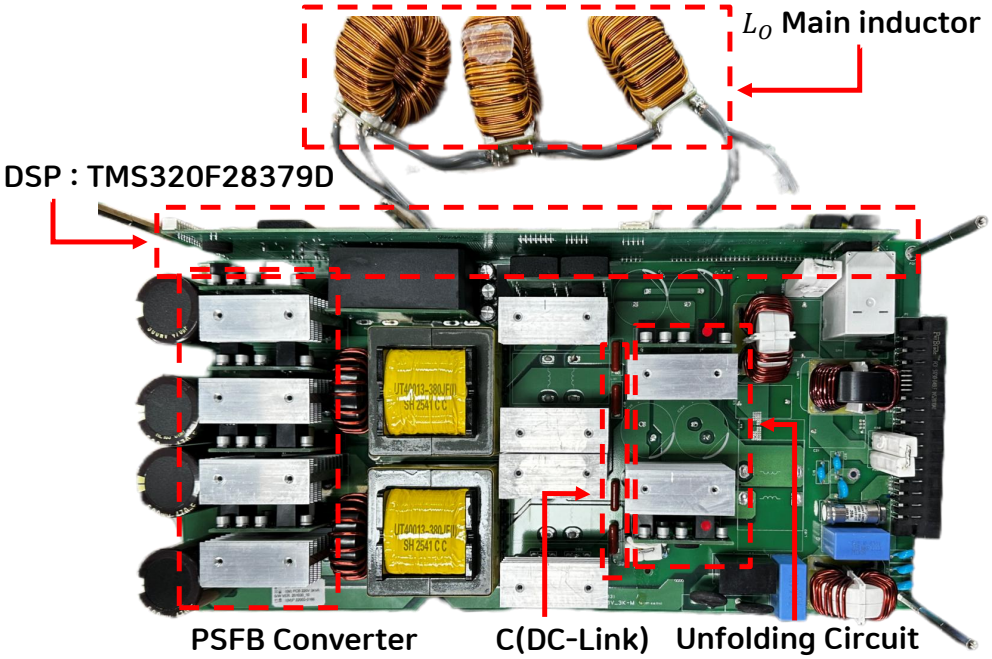
Open Loop THD : 19.3%
Close Loop THD : 0.41%

Harmonic Order	Frequency (Hz)	Open Loop Magnitude	Closed Loop Magnitude
3	180	34.01	0.166
5	300	25.02	0.118
7	420	20.06	0.115
9	540	18.30	0.099
11	660	15.56	0.088



Experimental Results and Verification

▪ Plant and parameters



Parameter	
V_{in}	$380V$
L_{lk}	$15\mu H$
L_m	$400\mu H$
L_o	$1.5mH$
C	$40nF$
R	16.13Ω(**Rated Load**) **3kVA**

▪ Experimental Main Waveform(5% Load 150W)

C1 : DC Link Voltage, C2 : Output Voltage , C4 : Duty

<Close Loop THD 0.8%>

<Open Loop THD 14.2%>

▪ At 5% load, THD was reduced from 14.2% to 0.8%.

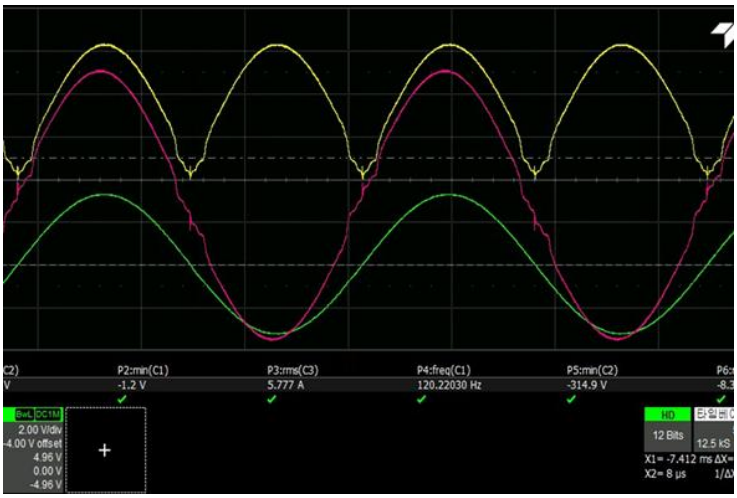
▪ Experimental Results and Verification

PEEC Laboratry

- Experimental Main Waveform(40% Load 1300W)

C1 : DC Link Voltage, C2 : Output Voltage , C4 : Duty

<Close Loop THD 0.9%>



<Open Loop THD 5.5%>

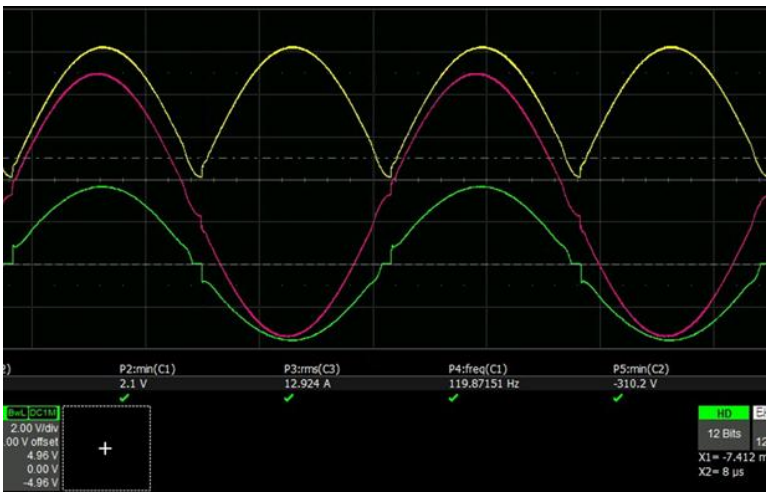
- At 40% load, THD was reduced from 5.5% to 0.9%.

▪ Experimental Results and Verification

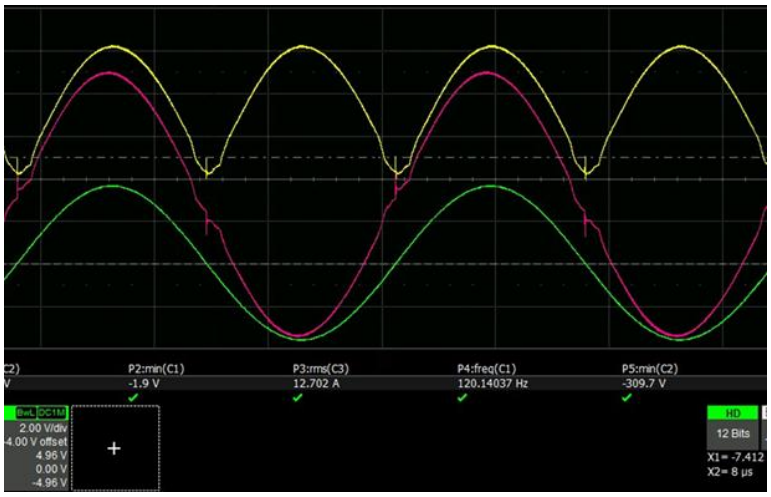
PEEC Laboratry

- Experimental Main Waveform(100% Load 3000W)

C1 : DC Link Voltage, C2 : Output Voltage , C4 : Duty



<Close Loop THD 1.1%>



<Open Loop THD 4.2%>

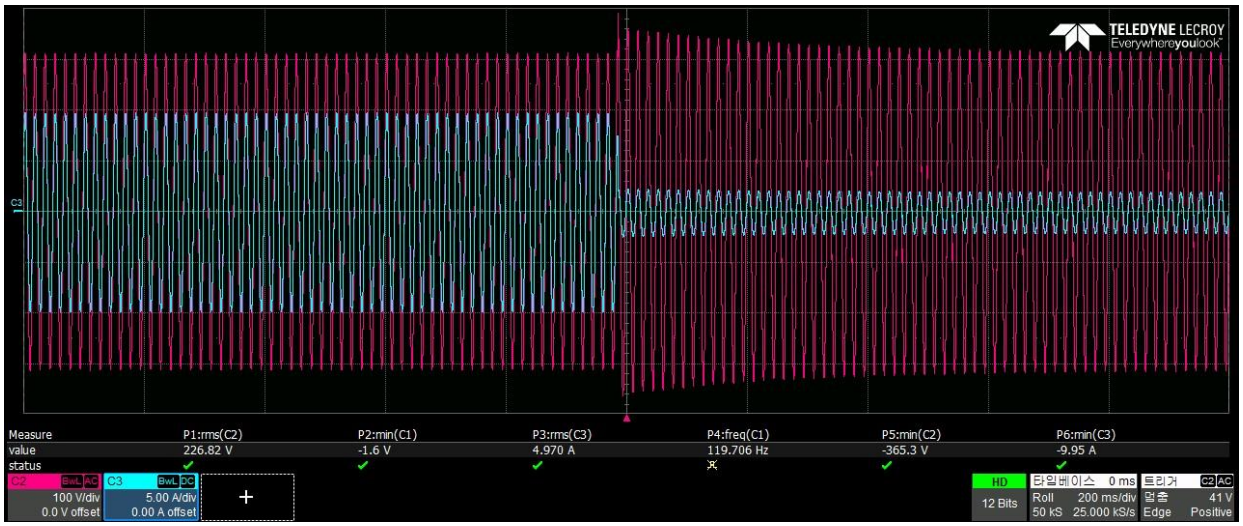
- At 100% load, THD was reduced from 1.1% to 4.2%.

▪ Experimental Results and Verification

PEEC Laboratry

- Load variation test

C2 : Output Voltage, C3 : Output Current

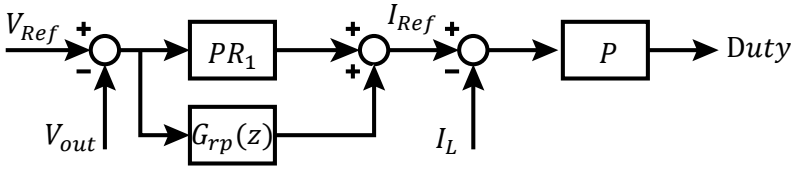


- 50%(1500W) -> 10%(300W) Load variation test
- Steady-state tracking takes more than 30 cycles

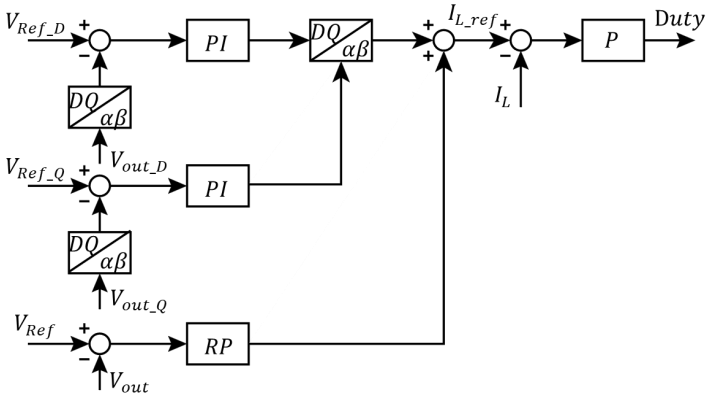
▪ Simulation Results and Control Method Comparison

PEEC Laboratry

- Control Method Change



< Proposed control method >

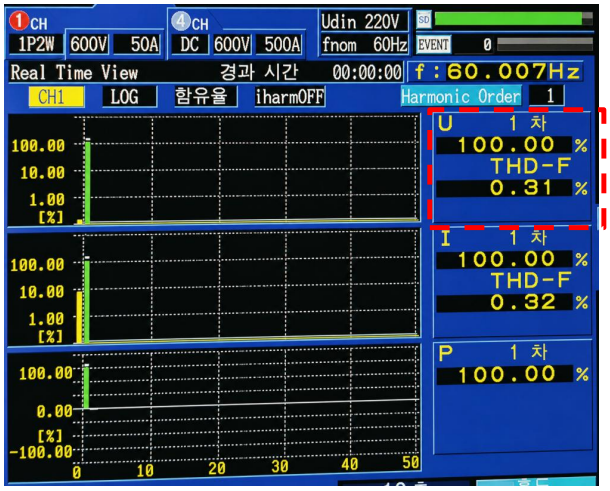


< A control method that compensates for load variations >

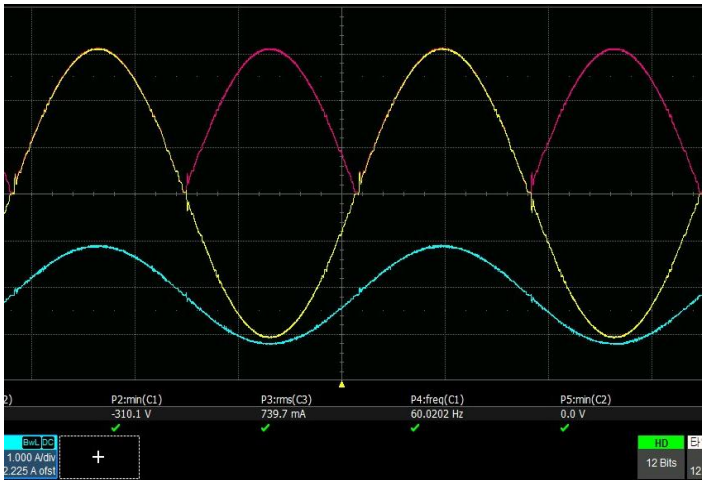
- The PR control was changed to single-phase DQ control to improve transient response during load variation.
- Since single-phase DQ control regulates DC quantities, it has lower control complexity, making gain tuning easier compared to PR control.
- In the proposed method, using RP on the DQ axis doubles the system memory capacity.

▪ Control method change(DQ-RP parallel)(5% Load 150W)

C1 : Output Voltage, C2 : DC Link Voltage , C3 : Output Current



<Power Quality Analyzer>

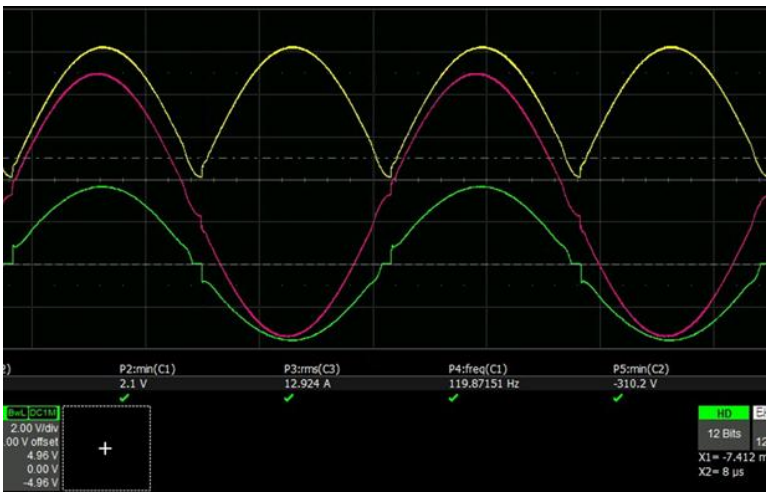


<DQ-RP THD 0.31%>

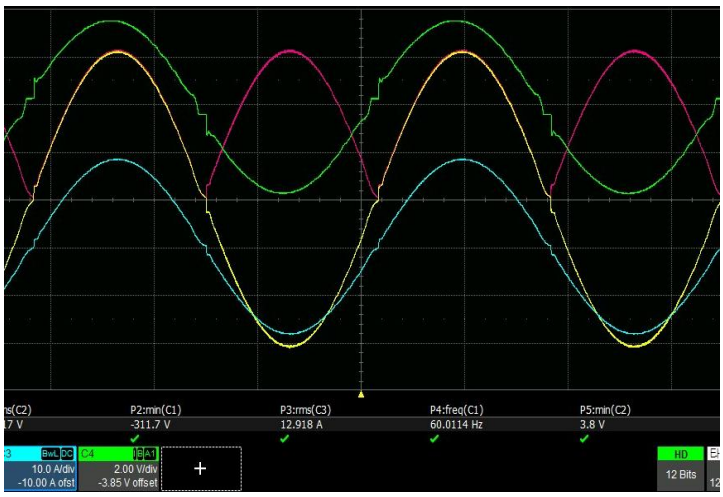
▪ Achieves THD of 0.31% at 5% load (Open-loop THD: 14.2%)

▪ Control method change(DQ-RP parallel)(100% Load 3000W)

C1 : DC Link Voltage, C2 : Output Voltage, C3 : Output Current, C4 : Duty



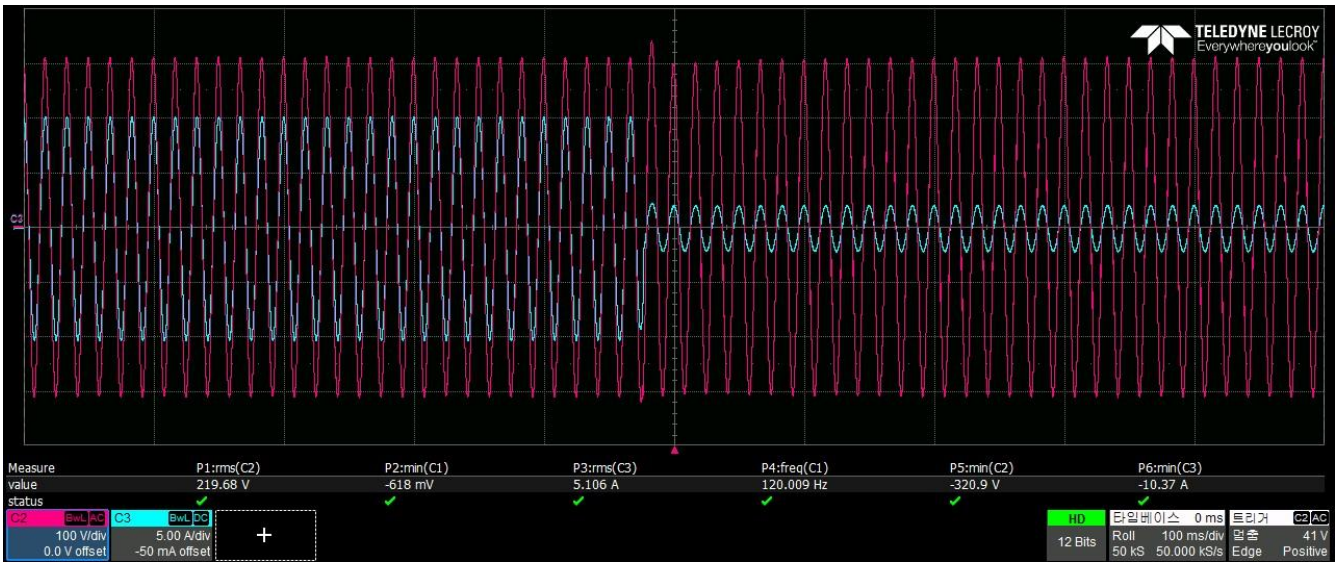
<PR-RP THD 1.1%>



<DQ-RP THD 0.69%>

▪ Achieves 95.1% efficiency at rated capacity

▪ Load variation test(DQ-RP parallel)



- 50%(1500W) -> 10%(300W) Load variation test
- Steady-state tracking takes more than 3 cycles

▪ Analytical Loss Analysis of Transformer and Inverter

		Loss Types	One	Total
PSFB Q1	Body Diode	Conduction Loss	1.64E-03	6.54E-03
	MOSFET		1.9615	7.846
	Body Diode	Switching Loss	6.67E-04	2.67E-03
	MOSFET		1.64983	6.59932
PSFB Q3	Body Diode	Conduction Loss	1.11E-03	4.44E-03
	MOSFET		2.04787	8.19148
	Body Diode	Switching Loss	1.80E-03	7.19E-03
	MOSFET		1.59156	6.36624
Diode 1		Conduction Loss	1.53	6.12
Diode 2		Conduction Loss	1.53	6.12
Unfolding Q1		Conduction Loss	2.59	10.36
		Switching Loss	2.73E-06	1.09E-05
			Total Loss	51.62W

Loss Items	Value
Transformer Core Loss P_{fe}	31.5W
Transformer Copper Loss P_{cu}	14.1W
Total Transformer Loss	45.6W
Two Transformers	91.2W
Inductor Core Loss P_{fe}	199.8mW
Inductor Copper Loss P_{cu}	505mW
Six Inductors	4.23W
System Total Loss	147.05W
Rated System Efficiency(25℃)	95.1%

Conclusion

▪ Conclusion

- The output voltage waveform distortion characteristics of a single-phase inverter based on an unfolding circuit were analyzed.
- It was confirmed that the zero-crossing interval is the primary distortion occurrence region, with switch transition and inductor current mode transition identified as the key causes.
- The proposed distortion reduction method (application of repetitive controller) was applied to improve the sinusoidal quality of the output voltage.
- By using RC (Repetitive Control), a simpler linear controller than the previously studied THD reduction techniques MPC and ILC, THD was effectively reduced.
- Through simulation and experimental results, a THD of less than 1% was achieved across the entire load range.
- The proposed isolated single-phase inverter achieved an efficiency of 95.1% under rated operation, confirming its performance and practical feasibility as a high-efficiency inverter.

Q & A

Appendix

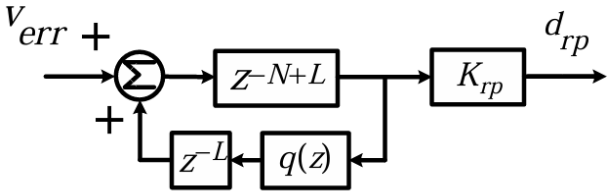
- Repetitive Controller Components

- The repetitive controller variables mainly consist of N, L, q(z), and Krp.

- $N = floor\left(\frac{fs}{fo}\right)$ ← floor(x) returns the largest integer less than or equal to x.
  - When N is a non-integer (decimal) value, the performance of the repetitive controller degrades.

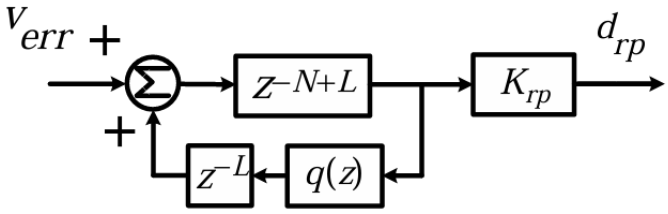
➢ $N = floor\left(\frac{fs}{fo}\right) = floor\left(\frac{75k}{60}\right) = 1250$
  - ➢ $(fs = 75kHz, f_o = 60Hz)$

- 1.5 sampling delay caused by the controller and PWM in digital control.
- L is a value that accounts for the sampling delay factor.
- Due to the 1.5 sampling delay, L is typically generalized as L = 2.

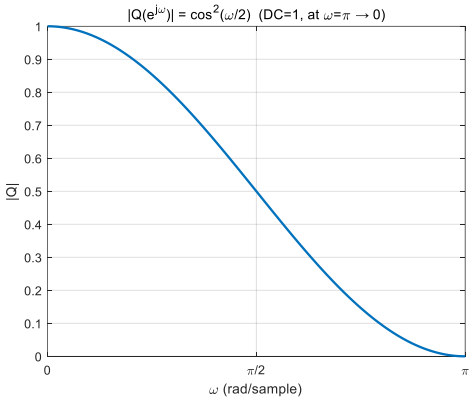


< Block Diagram of Grp(z) >

- q(z) Configuration



< Block Diagram of Grp(z) >



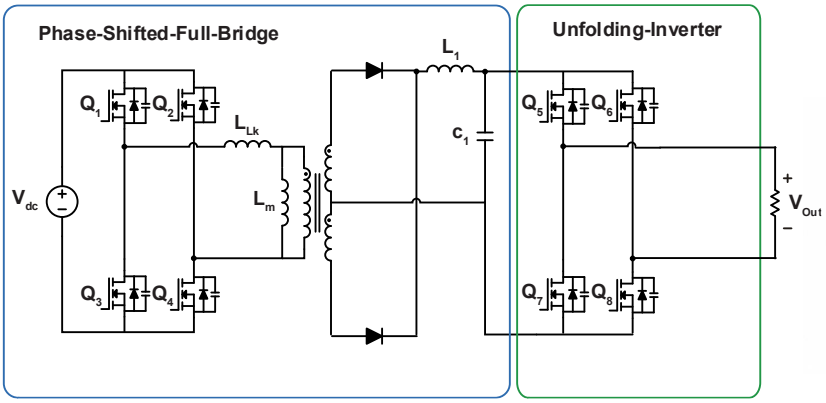
< Frequency Response of q(z) >

- $q(z) = \frac{z+2+z^{-1}}{4}$ or $0 < q(z) \leq 1$
- $(q(e^{jw}) = \frac{e^{jw}+2+e^{-jw}}{4} = \frac{1+\cos(\omega)}{2} = \cos^2(\frac{\omega}{2})$

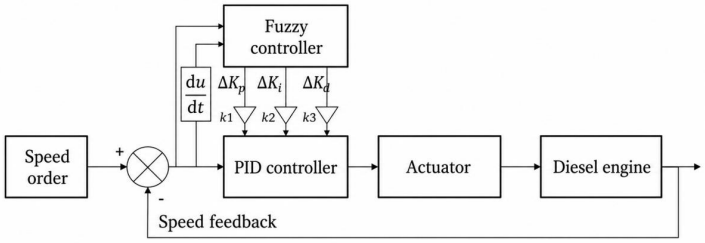
- A filter that attenuates the high gain of the repetitive controller in the high-frequency region.

▪ Parallel Structure of Fuzzy-PI Controller

Parameter	
L_1	$1.5mH$
C	$40nF$



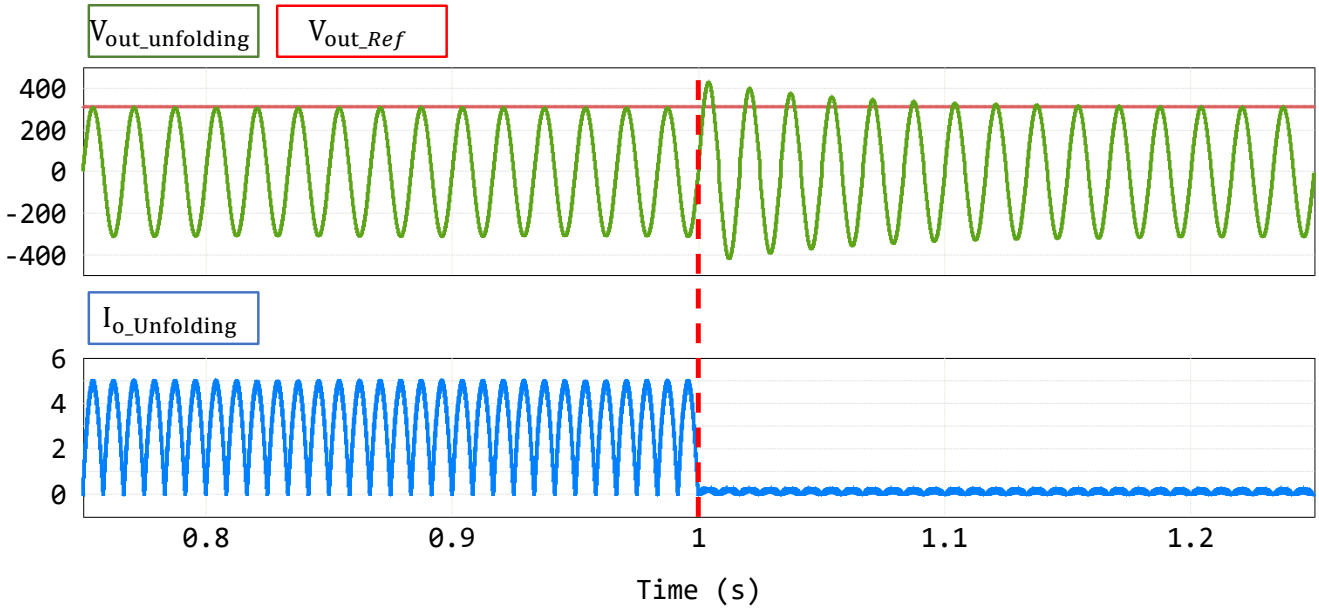
<PSFB-Unfolding Inverter>



<Block Diagram of Fuzzy-PI Control>

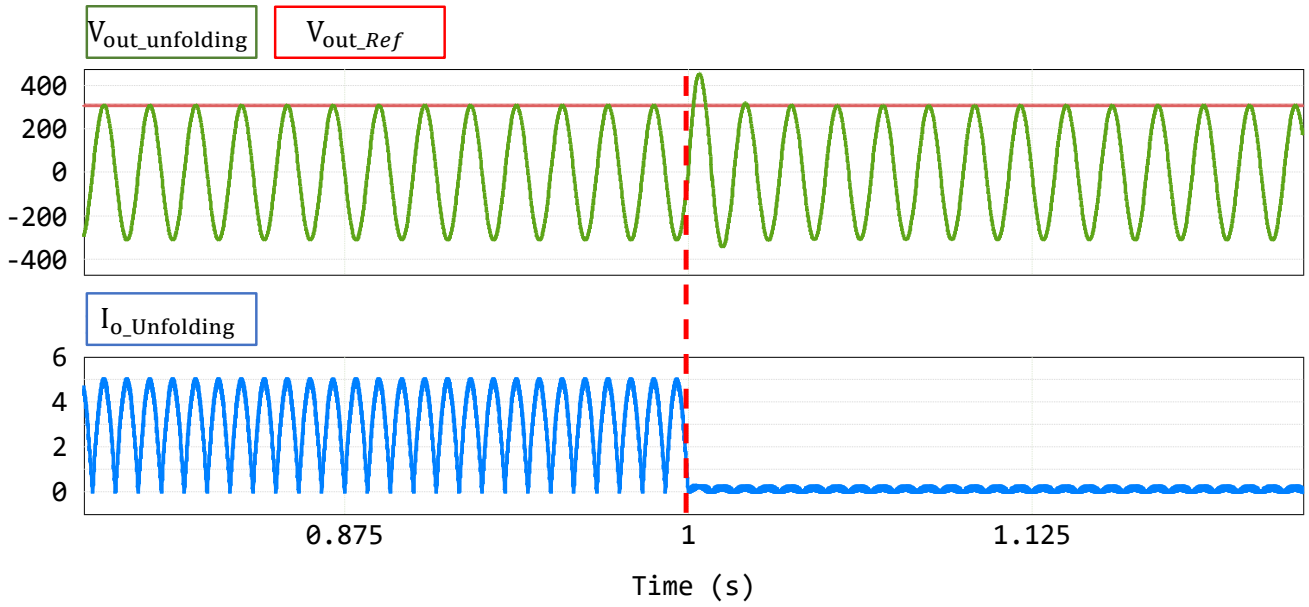
- $G_C(s) = K_P + \frac{K_I}{s} \rightarrow (K_P = K_{P0} + \triangle K_P \cdot k_1), (K_I = K_{I0} + \triangle K_I \cdot k_2)$
- $\triangle G_C(s) = K_{P0} + \triangle K_P \cdot k_1 + \frac{K_{I0} + \triangle K_I \cdot k_2}{s}$
- The Kp and Ki values are varied according to the magnitude of the error.

▪ Load Variation Simulation(PR-RP)(100 %Load -> 10% Load)



- Steady-state tracking takes more than 8 cycles

▪ Load Variation Simulation (DQ-RP)(100 %Load -> 10% Load)



▪ Steady-state tracking takes more than 2 cycles

Constant DC Current Control of Unidirectional High-Frequency Isolated Medium-Voltage AC-DC Modular Matrix Converter

Kohei Budo

6th Joint University Students Workshop (JUSW 2026)

May 14, 2026

Presented at the ICRERA 2024

[1]

Research Background

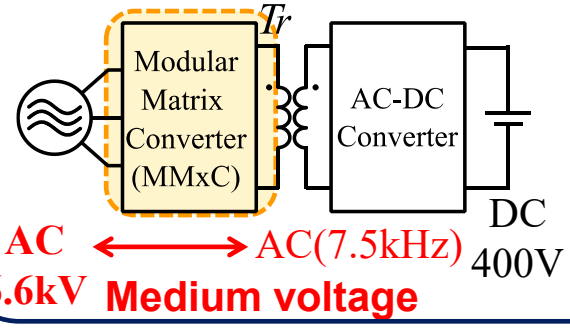
Electrical vehicles (EVs) are increasing toward carbon neutrality

Quick battery charger for high output power is being developed to reduce battery charge time for EVs

In quick battery charger,
Isolated AC-DC converter for high-power applications is used

Authors have proposed **isolated medium-voltage AC-DC converter using Modular Matrix Converter(MMxC)**

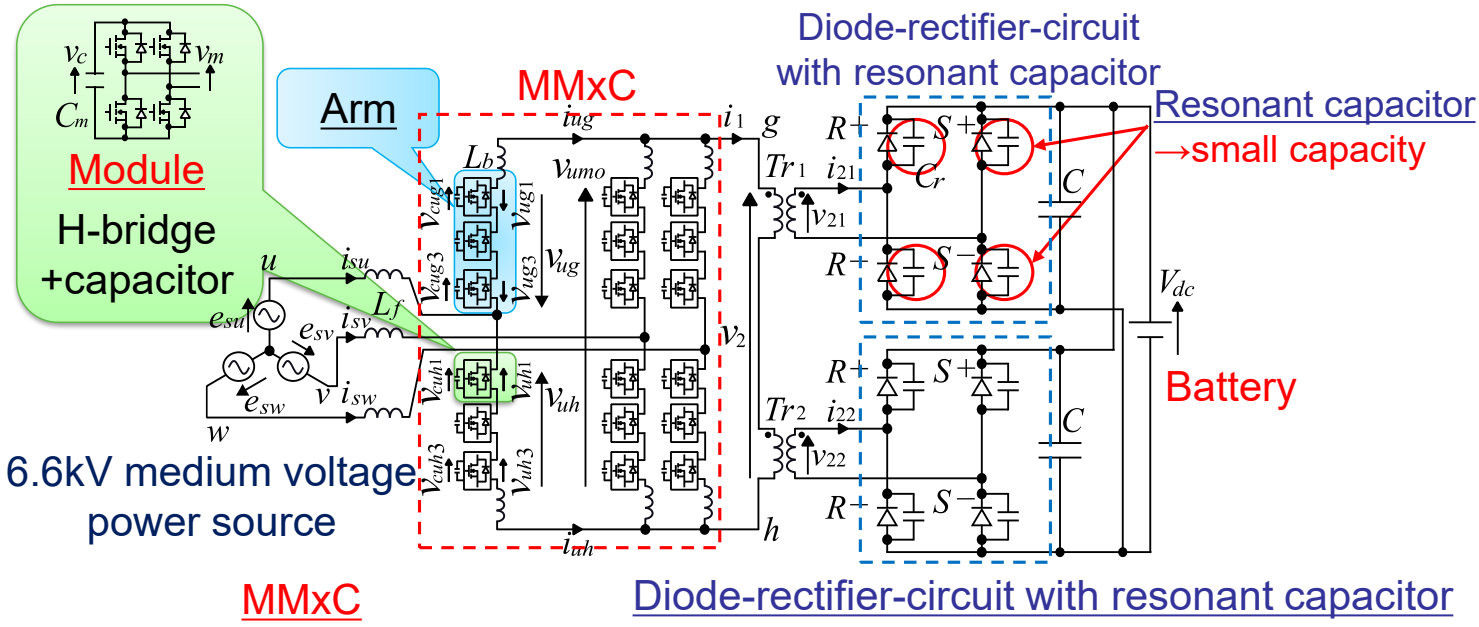
Proposed circuit



Feature

- Directly convert medium voltage power source by MMxC
- Achieve topology for high-power applications by input medium voltage
- Primary side composed by only MMxC
  →Downsized and high-efficient circuit

Circuit Configuration of Proposed Circuit



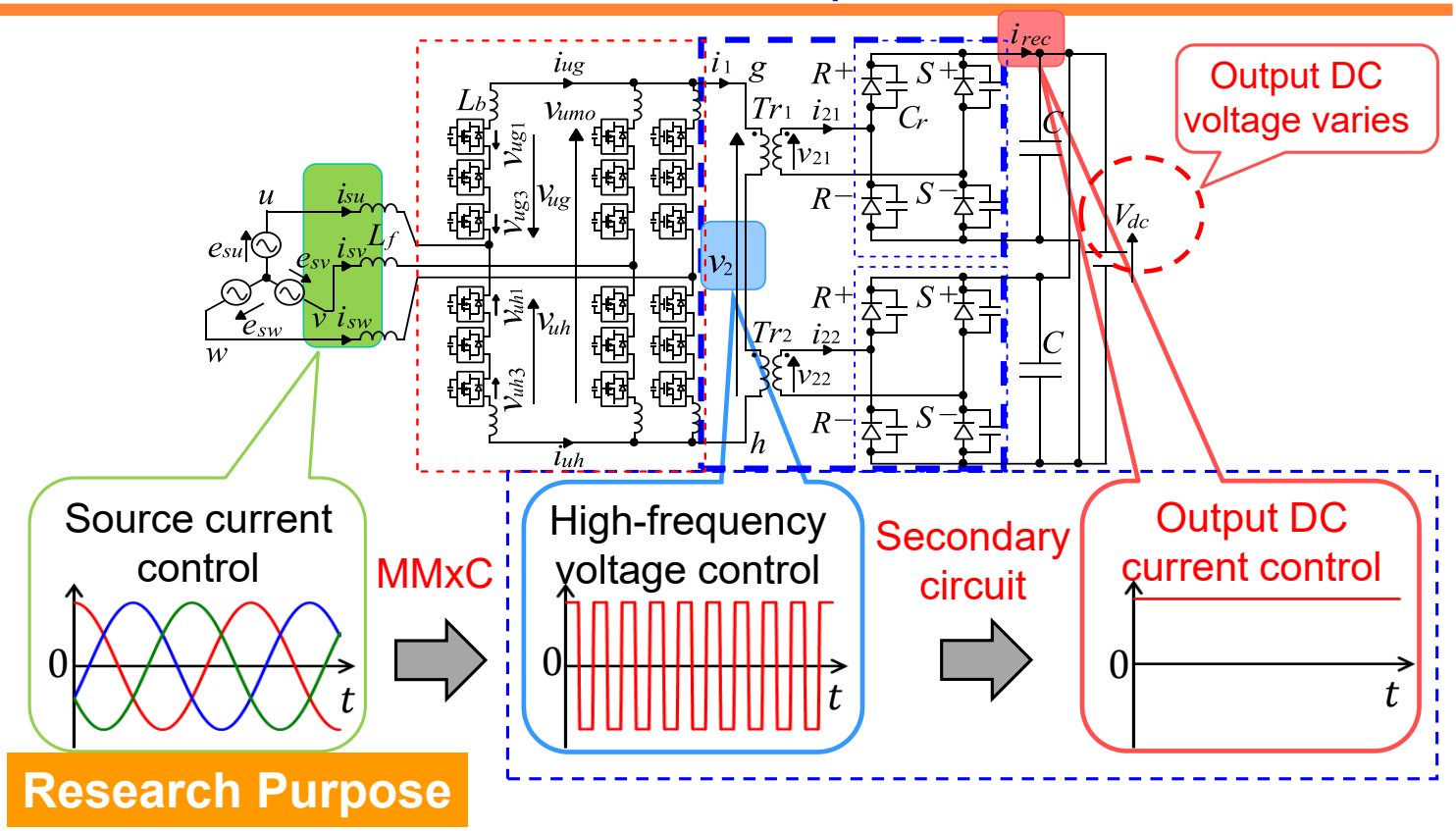
■ **Series connection of module**
Proposed circuit can achieve converter for high-power applications by input medium voltage.

■ **High total-power-factor of transformer**
by resonant capacitors
→Downsized high-frequency transformer

■ Parallel connection diode-rectifier-circuit

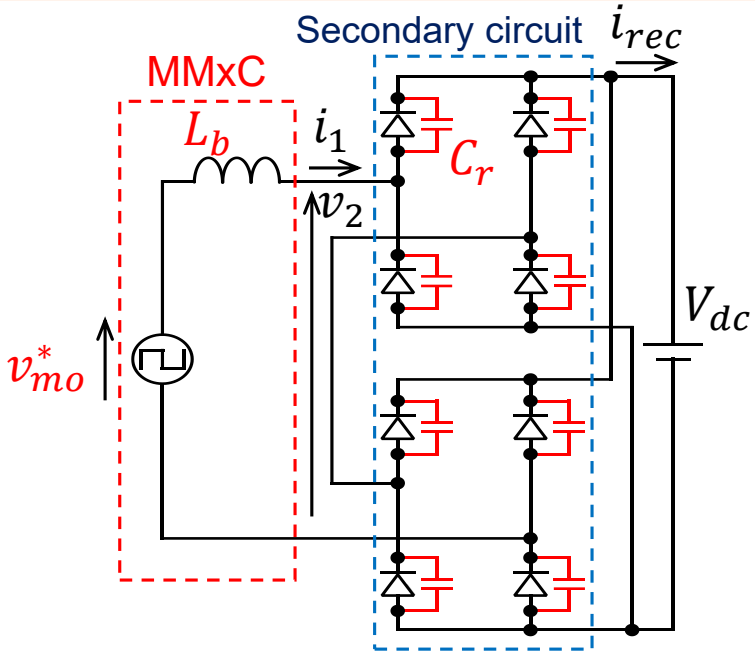
To achieve downsized and high-efficient circuit for high-power-applications

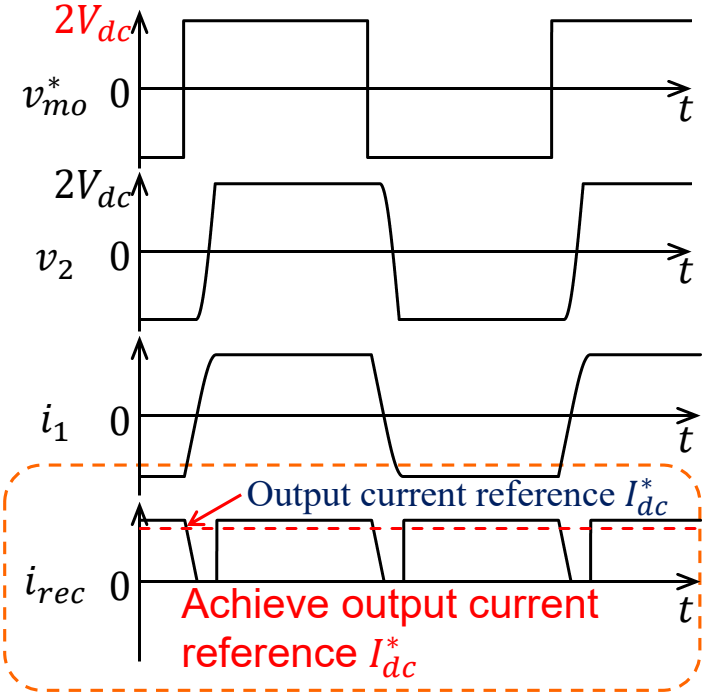
Control Method of Proposed Circuit and Research Purpose



Present output DC current control at any output DC voltage using high-frequency voltage generated by MMxC

High-Frequency Waveform at Rated Condition

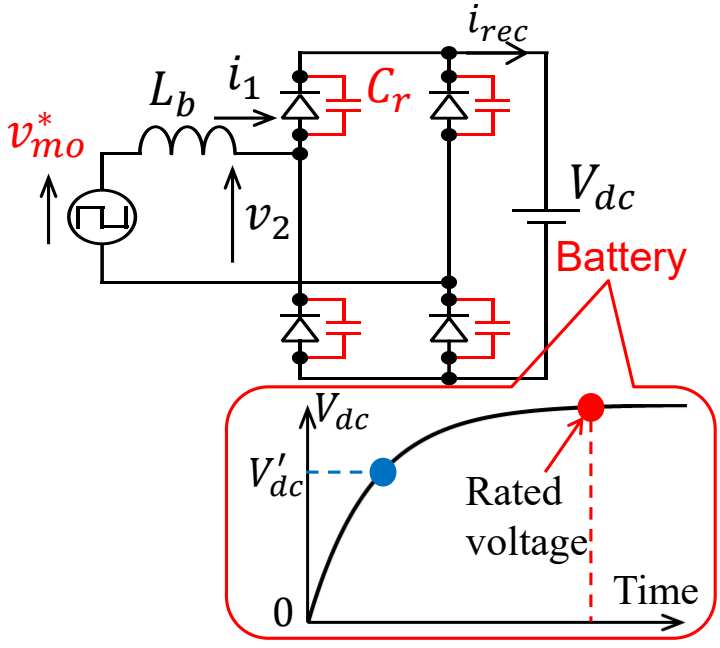




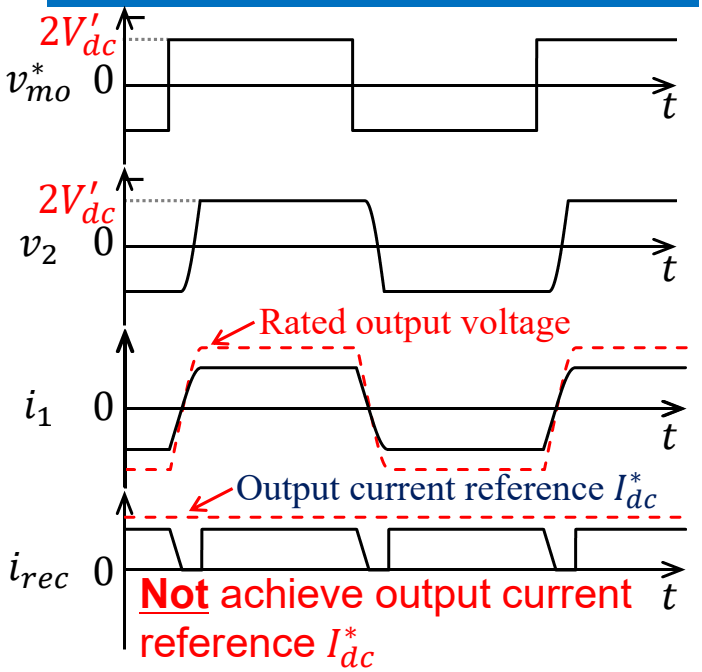
Control method and Feature

- Control amplitude of voltage v^*_{mo} equal to twice output DC voltage $2V_{dc}$
- DC current i_{rec} corresponding to DC current reference I^*_{dc} is acquired by design of resonant capacitor C_r
- High-frequency transformer is downsized by power factor correction

Research Purpose



Waveform at lower output DC voltage

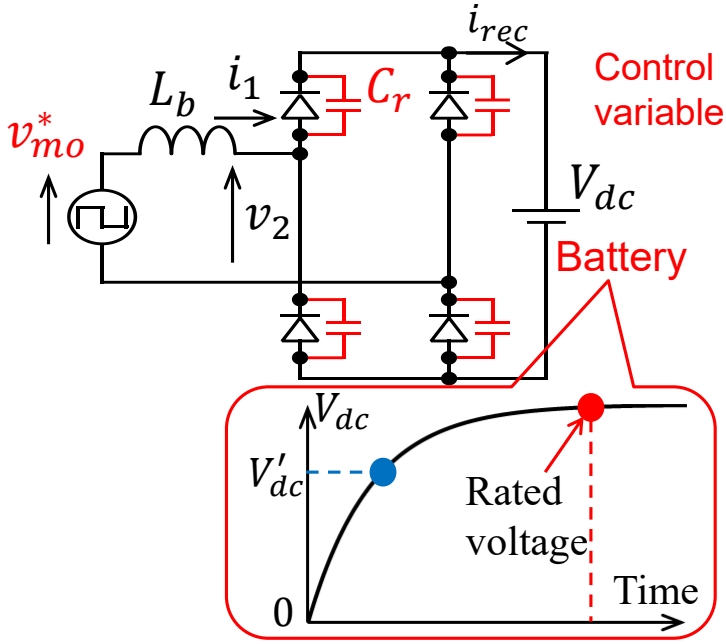


Research purpose

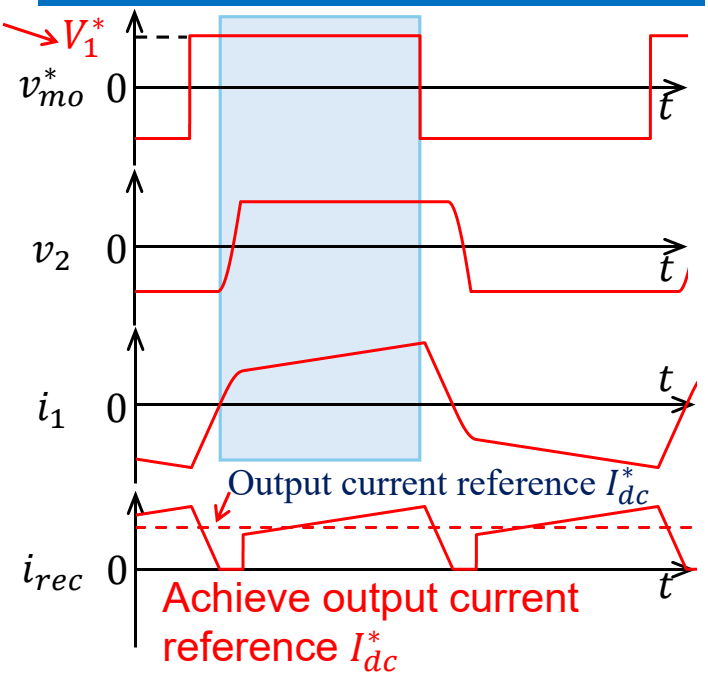
DC voltage V_{dc} varies by state of charge for battery
→Output current decreases due to low MMxC output voltage

Present output DC current control at any output DC voltage using amplitude of MMxC output voltage

Overview of Proposed Control Method



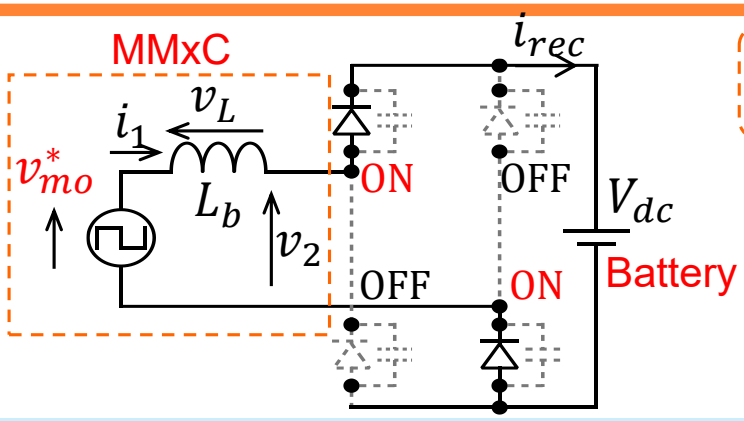
Waveform using proposed method



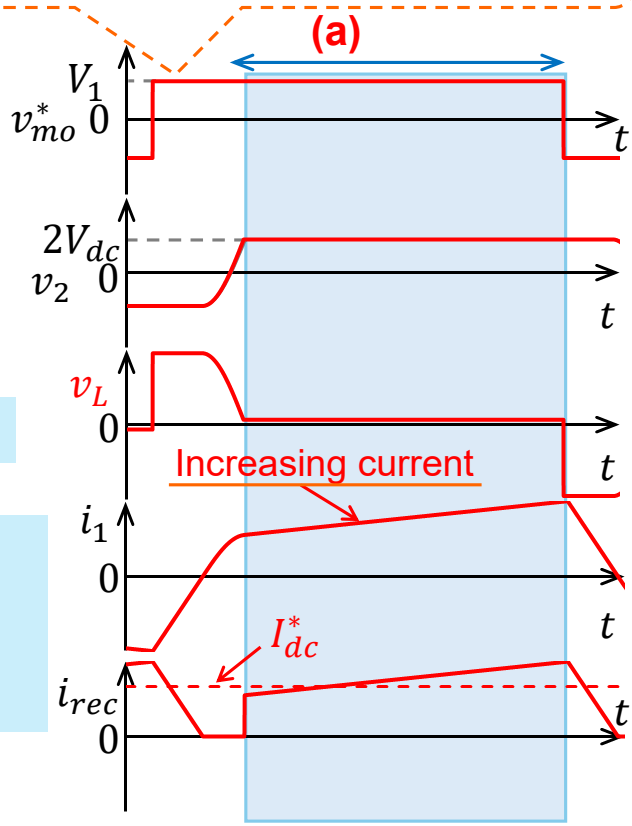
Feature of proposed method

- Realize **output DC current reference at any output DC voltage by using amplitude of MMxC output voltage v_{mo}**
- Using amplitude of MMxC output high-frequency voltage
  →Achieve stable operation of proposed circuit

Operating Principle of Proposed Method



Proposal
Higher amplitude than DC voltage $2V_{dc}$



Inductor voltage v_L is positive at (a) part

↓

Transformer current i_1 increases at (a) part

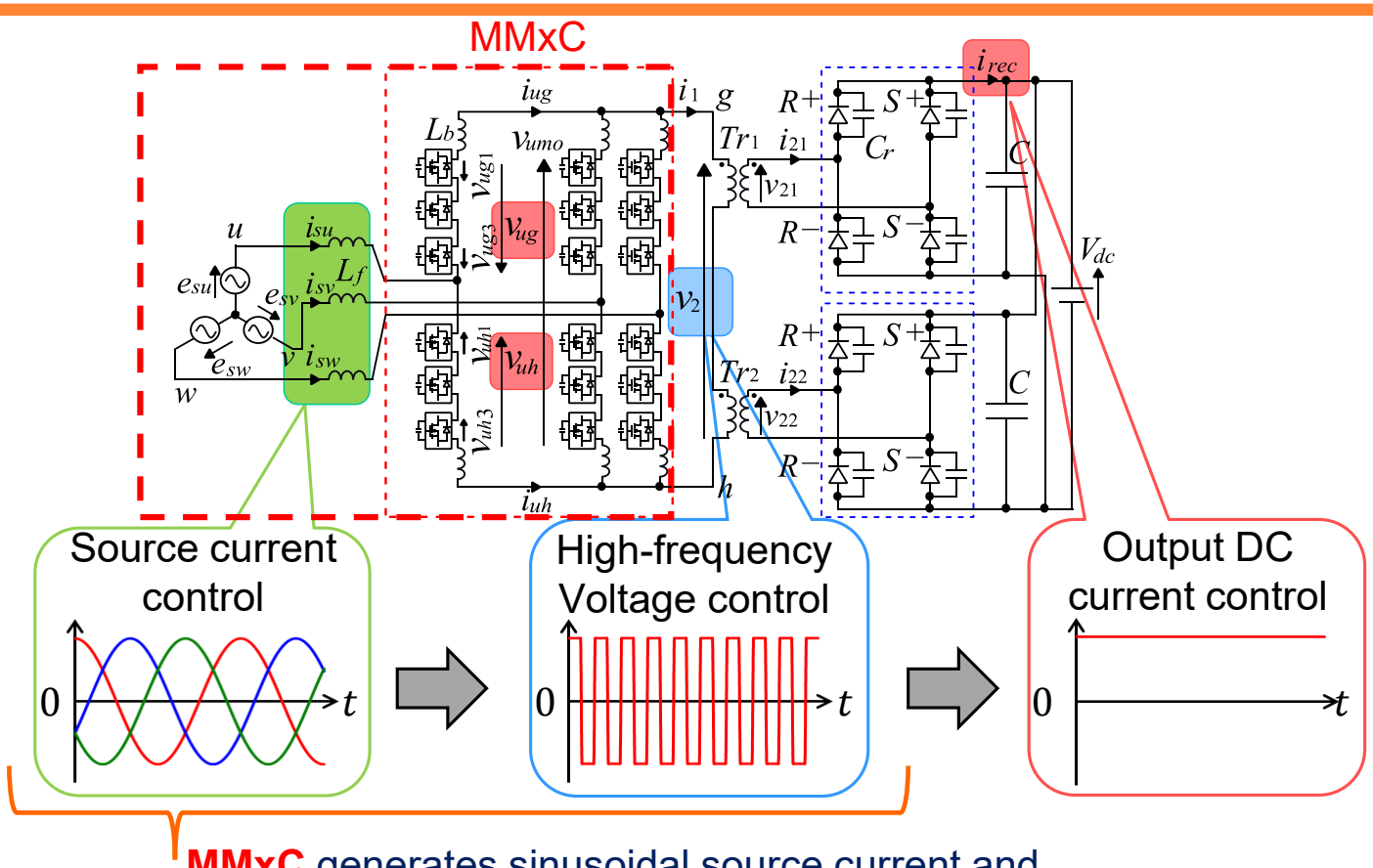
↓

Output current i_{rec} increases and is equivalently equal to current reference I_{dc}^*
→Control increasing amount of current i_1 by amplitude V_1 of MMxC output voltage

Calculate amplitude V_1 by PI controller to achieve output DC current reference

[8]

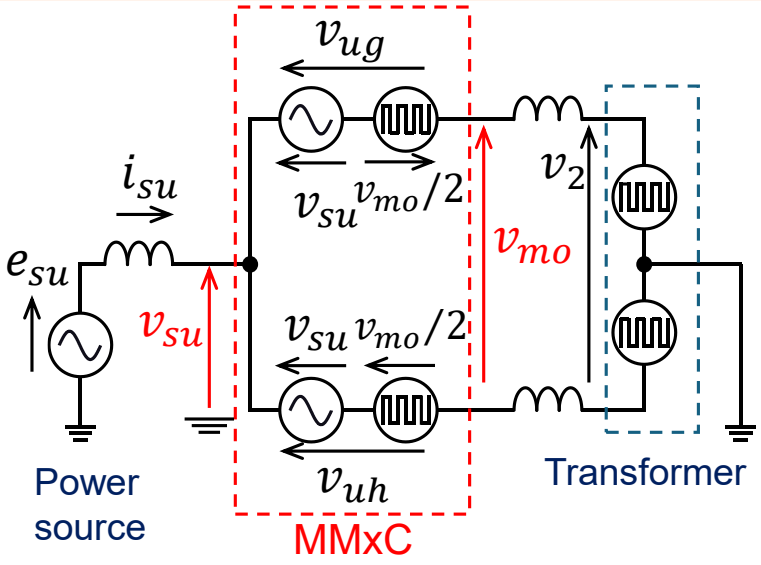
Generation Method of MMxC Output Voltage

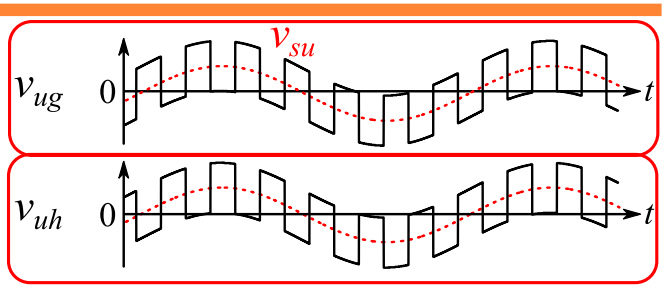


MMxC generates sinusoidal source current and high-frequency voltage at the same time using arm voltage v_{ug}, v_{uh}

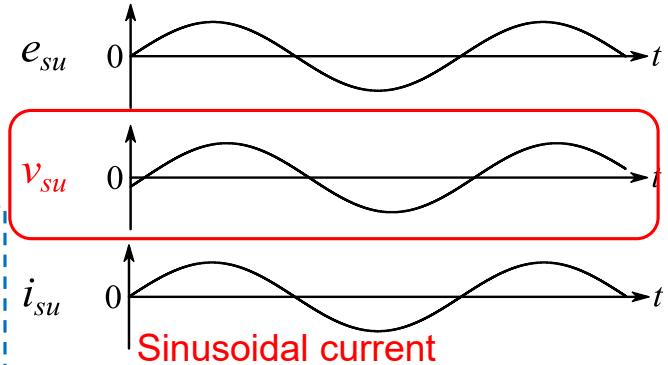
[9]

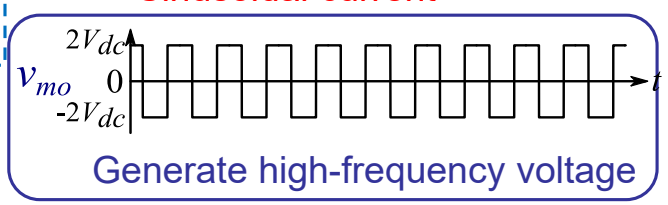
Operating Theory of MMxC





v_{su} : Sinusoidal voltage,
v_{mo} : High-frequency voltage

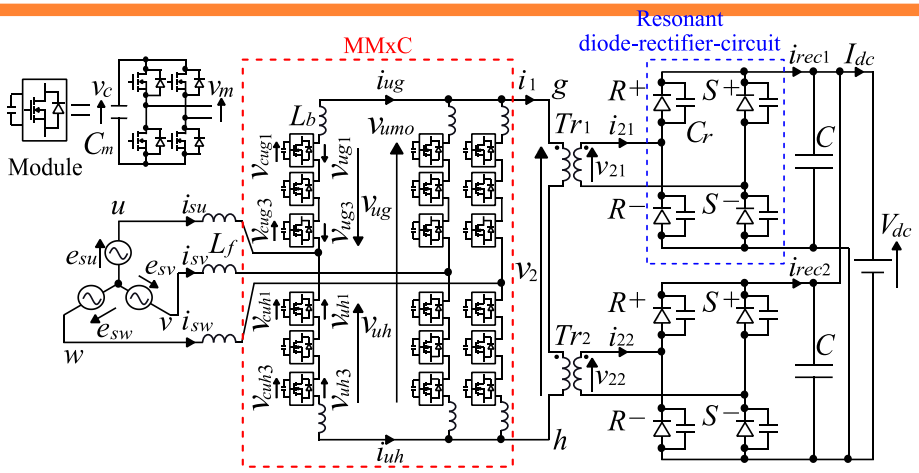




- Source current i_{su} is controlled by voltage $v_{su} = (v_{ug} + v_{uh})/2$
- High-frequency voltage v_{mo} is generated by voltage-difference $(v_{uh} - v_{ug})/2$

Achieve stable operation and output DC current reference by proposed method

Experimental Condition



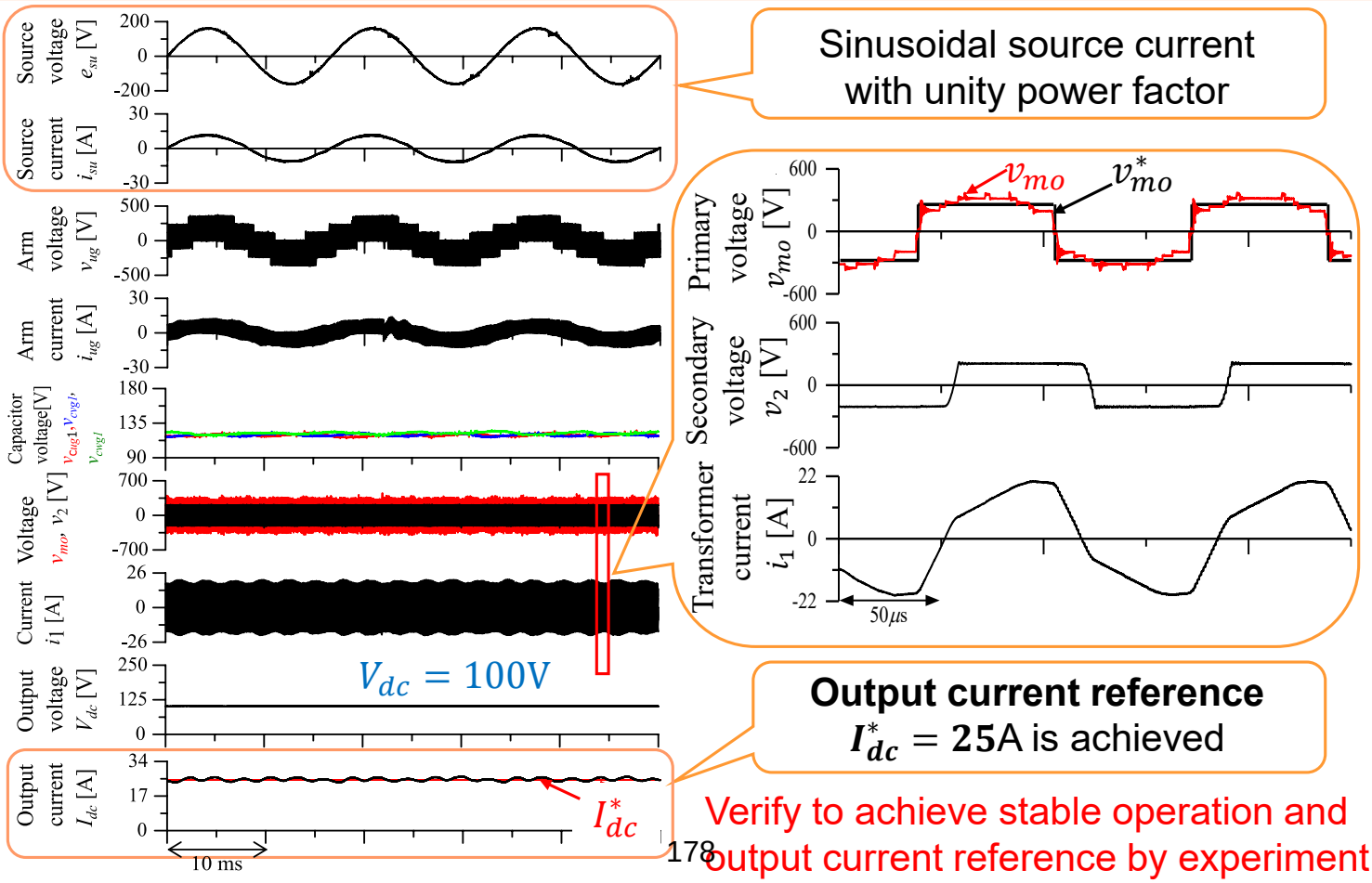
Source voltage E, ω	200 V, $2\pi \times 60$ rad/s	Module capacitor voltage $V_C{}^*$	145 V
Rated power P_r	6 kW	Turn ratio of transformer a	1
Inductance L_f , L_b	1.0 mH ,0.4 mH	Frequency of transformer $1/T_s$	7.5 kHz
Number of series modules n	3	Resonant capacitor C_r	150 nF
Number of transformers m	2	Output DC voltage V_{dc}	200 V
Module capacitors C_m	1200μF	**Output current reference I_{dc}^***	**25A**

Aim of experiments

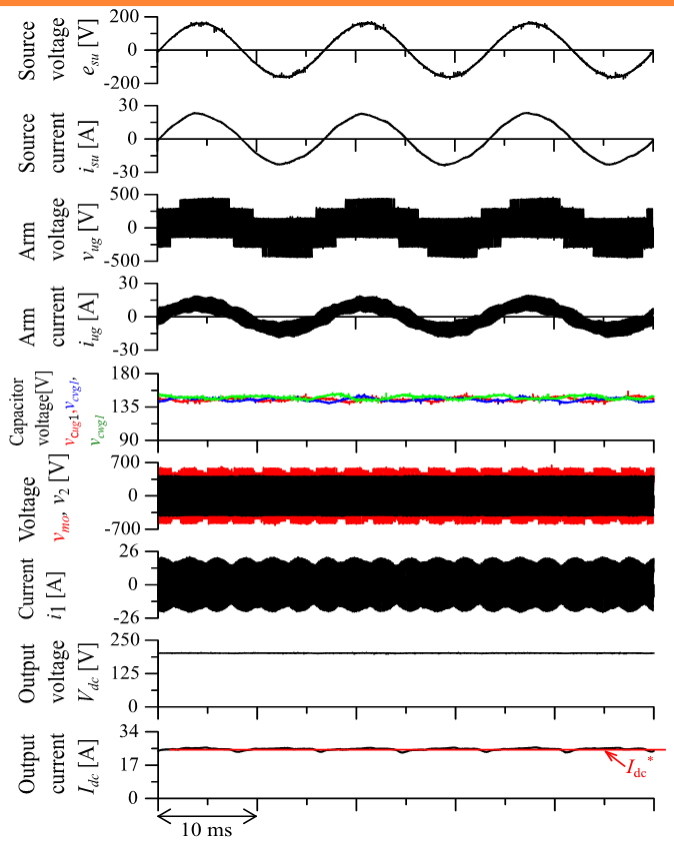
To achieve output DC current reference $I_{dc}^* = 25\text{A}$ using proposed control method in condition of output DC voltage $V_{dc} = 100,125,150,175,200\text{V}$.

Experimental Results at Output DC Voltage $V_{dc} = 100\text{V}$

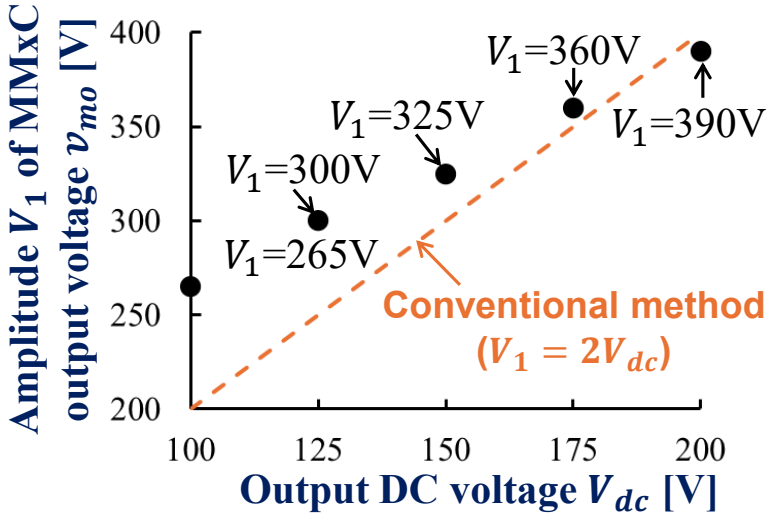
[11]



Experimental Results



Experimental waveform at $V_{dc} = 200\text{V}$



Experimental result

I calculated the appropriate amplitude V_1 of achieving output current reference $I_{dc}^* = 25\text{A}$ at five output DC voltage points ($V_{dc} = 100,125,150,175,200\text{V}$) by proposed control method

→Effectiveness of proposed method is verified

Conclusion

Research Purpose

This paper presents **constant output DC current control** for proposed isolated medium-voltage AC-DC modular matrix converter

Feature of Proposed Control Method

- Realize **output DC current reference at any output DC voltage**
- MMxC generates **source current with unity power factor** and **high-frequency voltage** at the same time

Achieve constant DC current control and stable and high-efficient operation of AC to DC conversion

Result

Verify the effectiveness of proposed control method by experiments using laboratory prototypes

Operation Analysis and Transfer Function Derivation of Three-Phase Unfolding Inverter for Renewable Energy

PEEC Laboratry

2026 Joint University Student Workshop

2026. 05.14

Presenter : Su Ho Park
Author : Su Ho Park, Eun Seop Kim, Hag Wone Kim†
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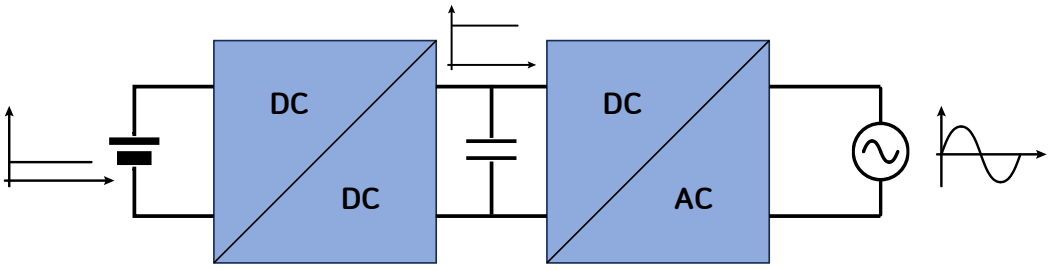
Table of Contents

PEEC Laboratry

Unfolding Circuit

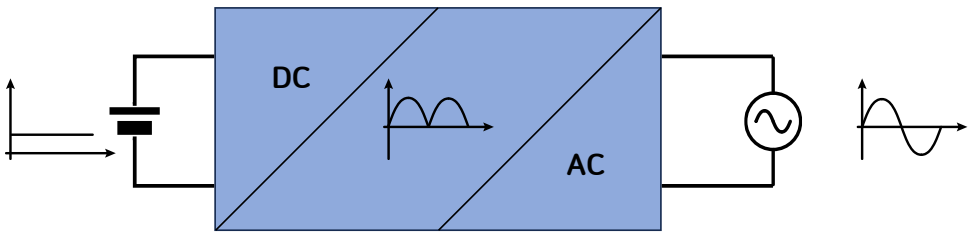
▪ Unfolding Circuit

▪ Basic Concept of the Unfolding Circuit



<General DC-AC conversion>

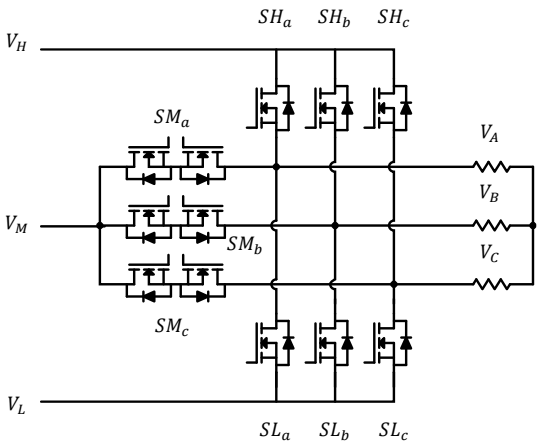
- General DC-AC conversion
  - ➢ Generally, both DC-DC converters and DC-AC inverters use PWM control for high-speed switching.



<DC-AC conversion using an unfolding circuit>

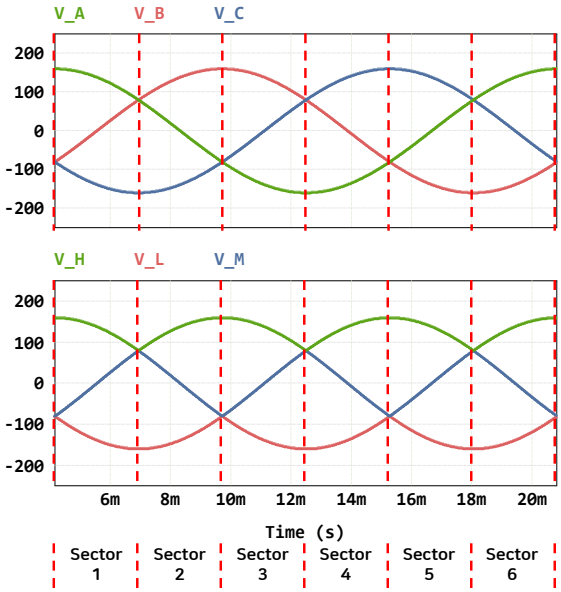
- DC-AC conversion using an unfolding circuit
  - ➢ The DC-DC converter performs high-speed switching using PWM control, while the unfolding circuit outputs AC through low-frequency switching without PWM control.

▪ Three Phase Unfolding Circuit



<Three Phase Unfolding Circuit>

	Sector					
	1	2	3	4	5	6
SH_a	1	0	0	0	0	1
SH_b	0	0	1	1	0	0
SH_c	0	1	0	0	1	0
SM_a	0	1	1	0	0	0
SM_b	0	0	0	0	1	1
SM_c	1	0	0	1	0	0
SL_a	0	0	0	1	1	0
SL_b	1	1	0	0	0	0
SL_c	0	0	1	0	0	1



- 3 switches per phase (High / Mid / Low)
- One line cycle = 6 sectors × 60°

Three Phase Unfolding Inverter Operation Analysis

▪ Three Phase Unfolding Inverter Operation Analysis

▪ Previous Research[1]

Voltage Control Method of Boost Integrated Bidirectional Three-Phase Inverter Based on Current Unfolding Topology

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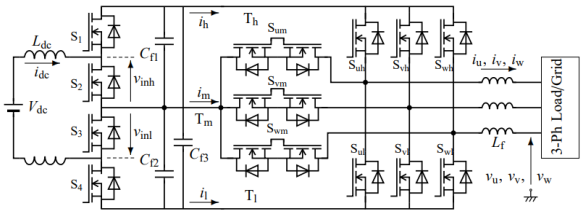


Fig. 1. Circuit diagram of the boost-integrated unfolding inverter.

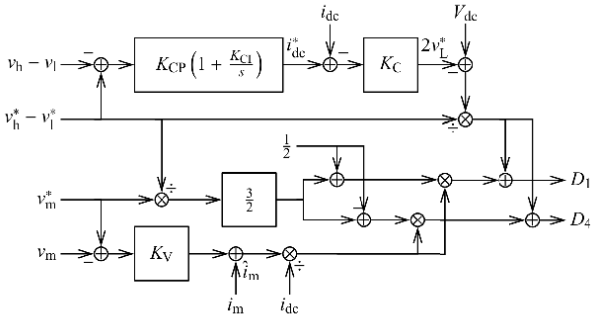


Fig. 4. Control block diagram of the three-phase battery inverter.

$$D_1 = \frac{V_{dc}-2v_L}{v_h-v_l} + \frac{v_h+2v_l}{v_h-v_l}\frac{i_m}{i_{dc}}, D_4 = \frac{V_{dc}-2v_L}{v_h-v_l} + \frac{2v_h+v_l}{v_h-v_l}\frac{i_m}{i_{dc}}$$

- Previous Research[1] esigned the controller using only static duty-ratio relations derived from KCL and KVL, without a small-signal transfer function model.
- This makes control-performance optimization and stability verification difficult, and limits controller redesign under parameter variations.

▪ Three Phase Unfolding Inverter Operation Analysis

▪ Previous Research [2]

12-2017

Bidirectional Three-Phase AC-DC Power Conversion Using DC-DC Converters and a Three-Phase Unfolder

Weilun Warren Chen
Utah State University

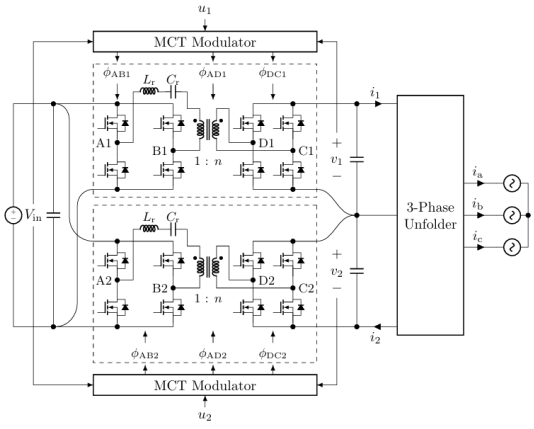
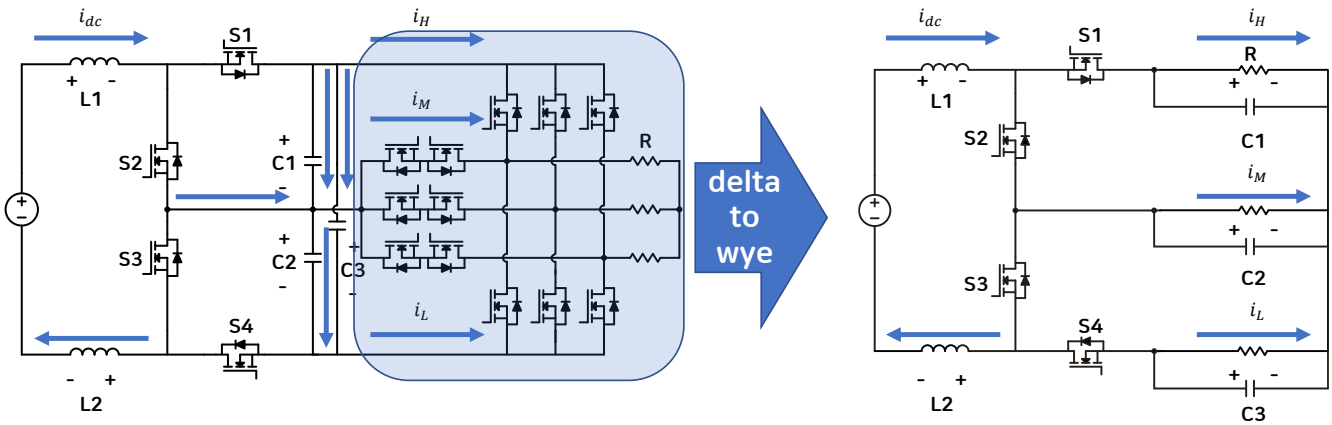


Fig. 3.11: MCT-modulated DBSRC modules with unfolder.

- Previous Research [2] generates the input voltages of the three-phase unfolding inverter using two resonant converters.
- Owing to its dual-converter structure, it suffers from lower power density and higher switching losses than a single-converter approach.
- This approach also lacks a small-signal transfer function model, making controller design difficult.

▪ Proposed Analysis of Three Phase Unfolding Inverter using Delta to Wye



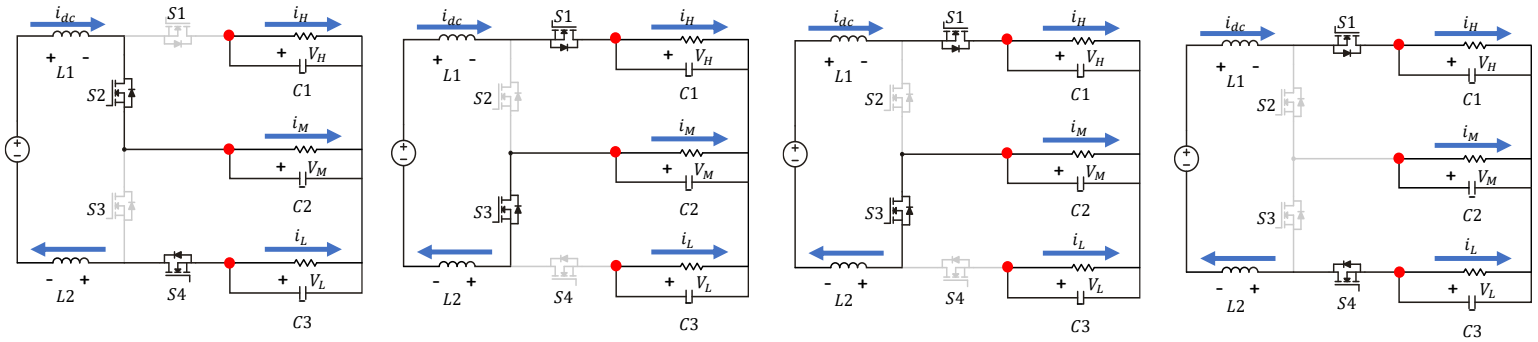
< Three Phase Unfolding Inverter Circuit>

<Simplified equivalent circuit>

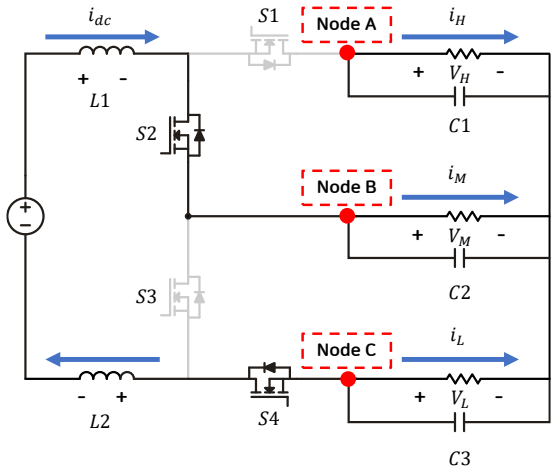
- The circuit with the T-type inverter involves many steps and is complex to analyze.
- Hence, the T-type is removed and the capacitor bank is reconfigured from delta to wye to derive the transfer function, yielding a simplified equivalent circuit.

▪ Mode Analysis

Mode1 Mode2 Mode3 Mode4



▪ Mode1 Model Equations

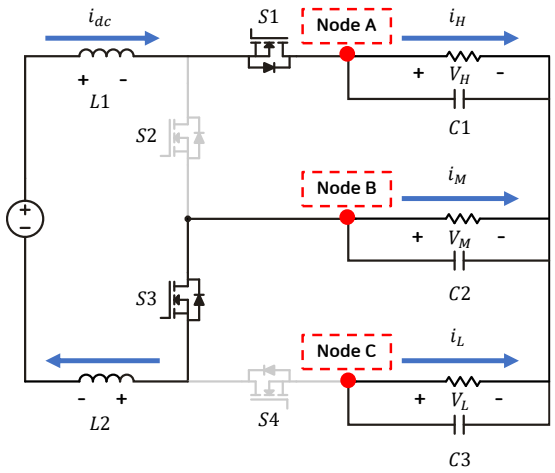


<Simplified equivalent circuit>

Conducting switches: S2, S4

- Node A (KCL)
  - $i_{C1} = -i_H$
  - $C1\frac{dV_{C1}}{dt} = -i_H = -\frac{V_H}{R}$
- Node B (KCL)
  - $i_{C2} = i_{S23} - i_M = i_{dc} - i_M$
  - $C2\frac{dV_{C2}}{dt} = i_{dc} - i_M = i_{dc} - \frac{V_M}{R}$
- Node C (KCL)
  - $i_{C3} = i_{S4} - i_L = -i_{dc} - i_L$
  - $C3\frac{dV_{C3}}{dt} = -i_{dc} - i_L = -i_{dc} - \frac{V_L}{R}$
- KVL including the voltage source
  - $2V_{L_{dc}} = V_{in} - V_M + V_L$
  - $\frac{di_{L_{dc}}}{dt} = \frac{V_{in}-V_M+V_L}{2L}$

▪ Mode2 Model Equations

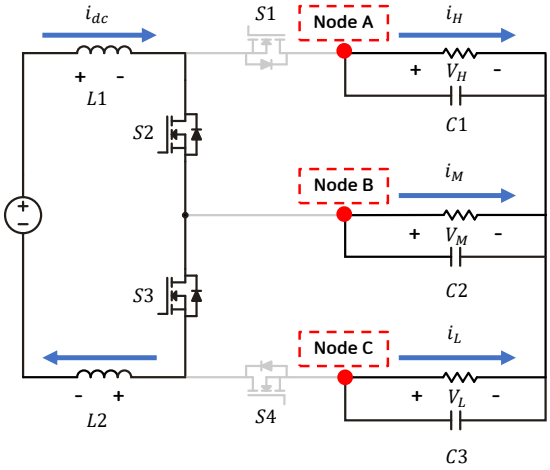


<Simplified equivalent circuit>

Conducting switches: S1, S3

- Node A (KCL)
  - $i_{C1} = i_{S1} - i_H = i_{dc} - i_H$
  - $C1\frac{dV_{C1}}{dt} = i_{dc} - i_H = i_{dc} - \frac{V_H}{R}$
- Node B (KCL)
  - $i_{C2} = i_{S23} - i_M = -i_{dc} - i_M$
  - $C2\frac{dV_{C2}}{dt} = -i_{dc} - i_M = -i_{dc} - \frac{V_M}{R}$
- Node C (KCL)
  - $i_{C3} = -i_L$
  - $C3\frac{dV_{C3}}{dt} = -i_L = -\frac{V_L}{R}$
- KVL including the voltage source
  - $2V_{L_{dc}} = V_{in} - V_H + V_M$
  - $\frac{di_{L_{dc}}}{dt} = \frac{V_{in}-V_H+V_M}{2L}$

▪ Mode3 Model Equations

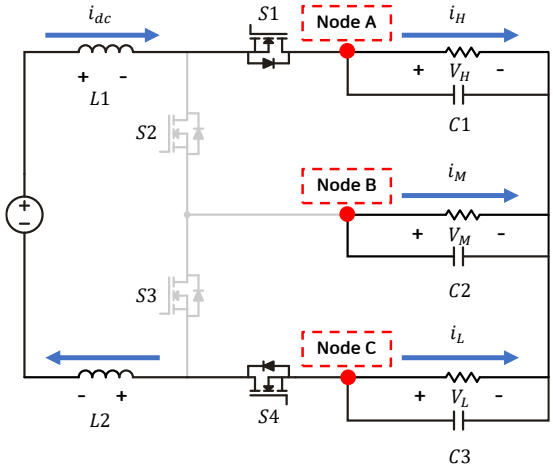


<Simplified equivalent circuit>

Conducting switches: S2, S3

- Node A (KCL)
  - $i_{C1} = -i_H$
  - $C1\frac{dV_{C1}}{dt} = -i_H = -\frac{V_H}{R}$
- Node B (KCL)
  - $i_{C2} = -i_M$
  - $C2\frac{dV_{C2}}{dt} = --i_M = -\frac{V_M}{R}$
- Node C (KCL)
  - $i_{C3} = -i_L$
  - $C3\frac{dV_{C3}}{dt} = -i_L = -\frac{V_L}{R}$
- KVL including the voltage source
  - $2V_{L_{dc}} = V_{in}$
  - $\frac{di_{L_{dc}}}{dt} = \frac{V_{in}}{2L}$

▪ Mode4 Model Equations

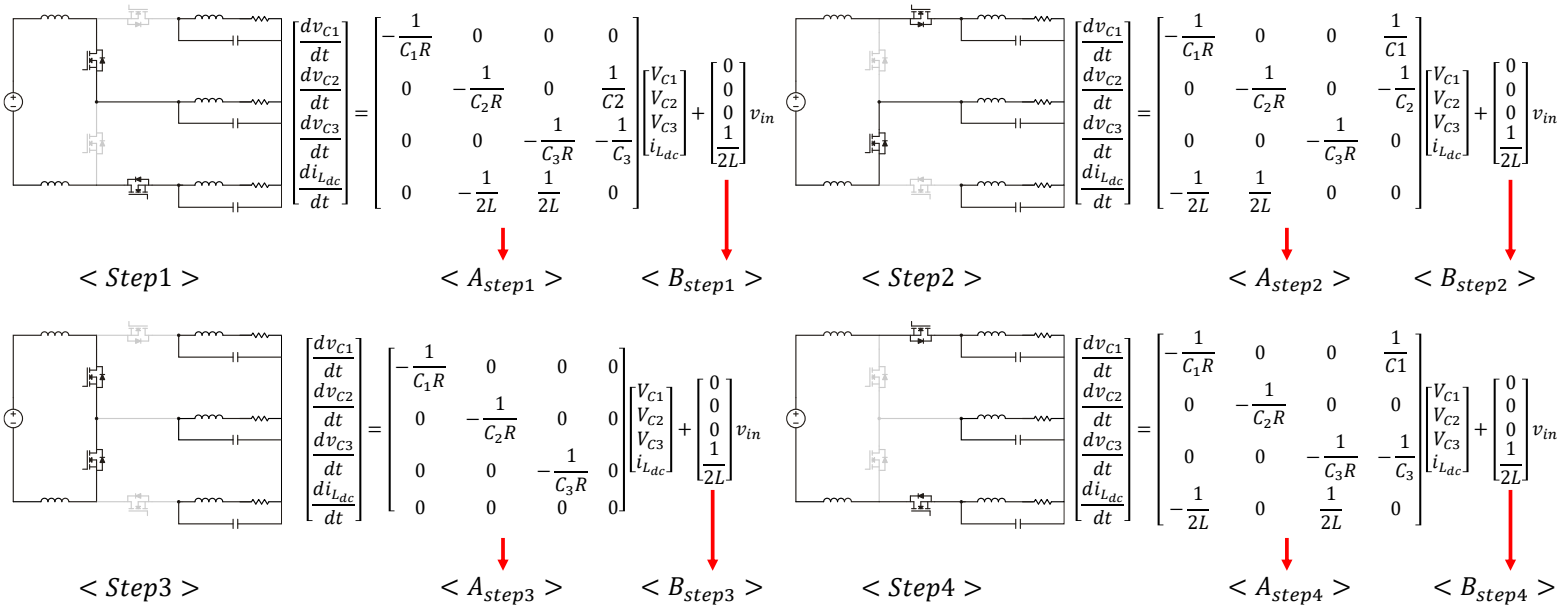


<Simplified equivalent circuit>

Conducting switches: S1, S4

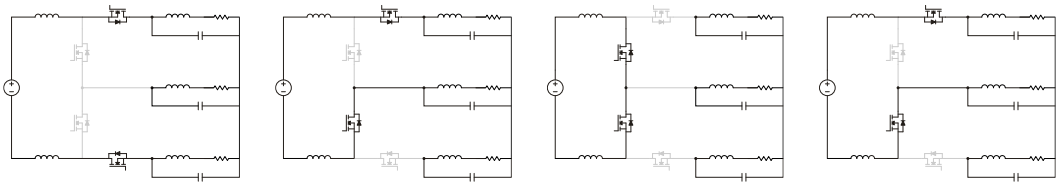
- Node A (KCL)
  - $i_{C1} = i_{S1} - i_H = i_{dc} - i_H$
  - $C1\frac{dV_{C1}}{dt} = i_{dc} - i_H = i_{dc} - \frac{V_H}{R}$
- Node B (KCL)
  - $i_{C2} = -i_M$
  - $C2\frac{dV_{C2}}{dt} = --i_M = -\frac{V_M}{R}$
- Node C (KCL)
  - $i_{C3} = i_{S4} - i_L = -i_{dc} - i_L$
  - $C3\frac{dV_{C3}}{dt} = -i_{dc} - i_L = -i_{dc} - \frac{V_L}{R}$
- KVL including the voltage source
  - $2V_{L_{dc}} = V_{in} - V_H + V_L$
  - $\frac{di_{L_{dc}}}{dt} = \frac{V_{in}-V_H+V_L}{2L}$

- State Equations by Step



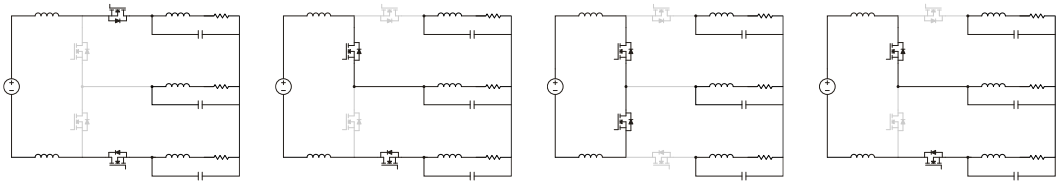
- State-Space Averaging of the A Matrix by Mode

mode1



$D4$ $(D1-D4)/2$ $1-D1$ $(D1-D4)/2$

mode2



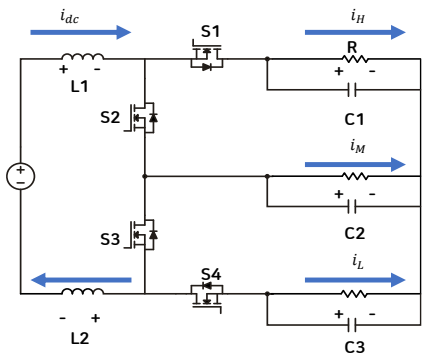
$D1$ $(D4-D1)/2$ $1-D4$ $(D4-D1)/2$

- 4 steps → grouped into 2 operating modes
- Mode classification by capacitor voltages
- Both modes yield the same averaged A matrix

- A_{AVg}

$$\begin{bmatrix} -\frac{1}{C_1R} & 0 & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_2R} & 0 & \frac{D4-D1}{C2} \\ 0 & 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ -\frac{D1}{2L} & -\frac{D1-D4}{2L} & \frac{D4}{2L} & 0 \end{bmatrix}$$

▪ Voltage Conversion Ratio

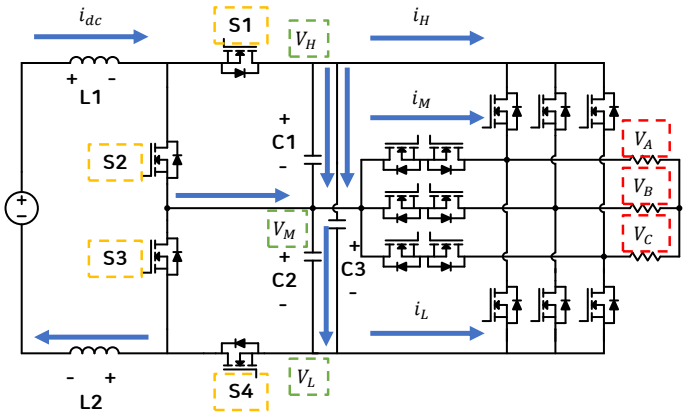


<Simplified equivalent circuit>

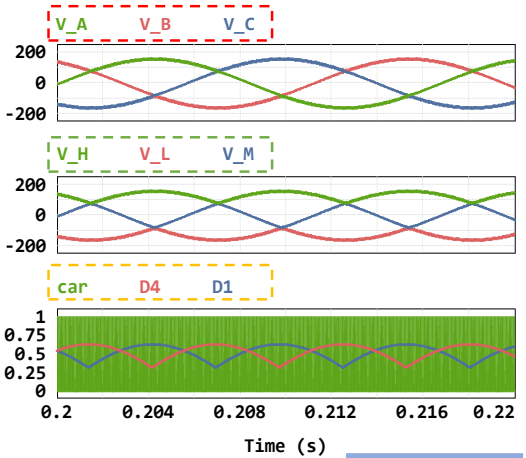
- $\frac{dv_{C1}}{dt} = -\frac{v_H}{C_1 R} + \frac{D1}{C_1} i_{dc}$
- $\frac{dv_{C2}}{dt} = -\frac{v_M}{C_2 R} + \frac{D4-D1}{C2} i_{dc}$
- $\frac{dv_{C3}}{dt} = -\frac{v_L}{C_3 R} - \frac{D4}{C_3} i_{dc}$
- $\frac{di_{L_{dc}}}{dt} = \frac{v_{in}}{2L} - \frac{D1}{2L} v_H - \frac{D1-D4}{2L} v_M + \frac{D4}{2L} v_L$

- One-cycle averaging → steady-state operating point
  - $0 = -\frac{V_H}{R} + D1 * I_{dc}$
  - $0 = -\frac{V_M}{R} + (D4 - D1) * I_{dc}$
  - $0 = -\frac{V_L}{R} - D4 * I_{dc}$
  - $0 = V_{in} - D1 * V_H - (D1 - D4)V_M + D4V_L \cdots (a)$
- Organize into V_H, V_M, V_L
  - $V_H = R * D1 * I_{dc} \cdots (1)$
  - $V_M = R * (D4 - D1) * I_{dc} \cdots (2)$
  - $V_L = -R * D4 * I_{dc} \cdots (3)$
- Substitute (1), (2), and (3) into (a)
  - $I_{dc} = \frac{V_{in}}{R*(D1^2+(D1-D4)^2+D4^2)} \cdots (4)$
- Substitute (4) into (1), (2), and (3) respectively
  - $\frac{V_H}{V_{in}} = \frac{D1}{D1^2+(D1-D4)^2+D4^2}$
  - $\frac{V_M}{V_{in}} = \frac{D4-D1}{D1^2+(D1-D4)^2+D4^2}$
  - $\frac{V_L}{V_{in}} = -\frac{D4}{D1^2+(D1-D4)^2+D4^2}$

▪ Open-Loop Simulation Result / THD = 2 %



< Three Phase Unfolding Inverter Circuit>



- Open-loop duty D computed from the voltage conversion ratio (Slide 15)
- Output voltage THD ≈ 2 %

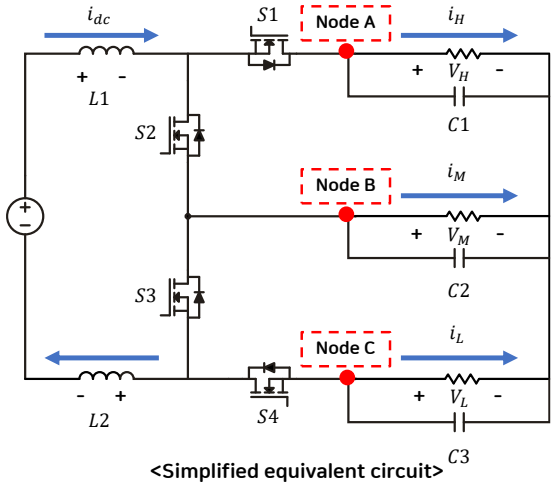
- $\frac{V_H}{V_{in}} = \frac{D1}{D1^2+(D1-D4)^2+D4^2}$
- $\frac{V_M}{V_{in}} = \frac{D4-D1}{D1^2+(D1-D4)^2+D4^2}$
- $\frac{V_L}{V_{in}} = -\frac{D4}{D1^2+(D1-D4)^2+D4^2}$

Parameter	
C_1	$1\mu F$
C_2	$1\mu F$
C_3	$1\mu F$
f_{sw}	$60kHz$

Three Phase Unfolding Inverter Transfer Function Derivation

PEEC Laboratry

▪ Small-Signal Modeling of the Three-Phase Unfolding Inverter



<Simplified equivalent circuit>

- 4×4 model: too complex for tractable analysis
- V_{C2} can be expressed via V_{C1} and V_{C3}
- Reduced to a 3×3 model for transfer-function derivation

- State averaging equation

$$\begin{bmatrix} \frac{dv_{C1}}{dt} \\ \frac{dv_{C3}}{dt} \\ \frac{di_{L_{dc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1 R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3 R} & -\frac{D4}{C_3} \\ \frac{D4-2*D1}{2L} & \frac{2*D4-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C3} \\ i_{L_{dc}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2L} \end{bmatrix} v_{in}$$

- Small-signal modeling

$$\begin{bmatrix} \frac{d(V_{C1}+\widehat{v_{C1}})}{dt} \\ \frac{d(V_{C3}+\widehat{v_{C3}})}{dt} \\ \frac{d(I_{Ldc}+\widehat{i_{Ldc}})}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1 R} & 0 & \frac{D1+\widehat{d1}}{C_1} \\ 0 & -\frac{1}{C_3 R} & -\frac{D4}{C_3} \\ \frac{D4-2*(D1+\widehat{d1})}{2L} & \frac{2*D4-(D1+\widehat{d1})}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_{C1}+\widehat{v_{C1}} \\ V_{C3}+\widehat{v_{C3}} \\ I_{Ldc}+\widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2L} \end{bmatrix} v_{in}$$

$$\begin{bmatrix} \frac{d(V_{C1}+\widehat{v_{C1}})}{dt} \\ \frac{d(V_{C3}+\widehat{v_{C3}})}{dt} \\ \frac{d(I_{Ldc}+\widehat{i_{Ldc}})}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1 R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3 R} & -\frac{D4+\widehat{d4}}{C_3} \\ \frac{D4+\widehat{d4}-2*D1}{2L} & \frac{2*(D4+\widehat{d4})-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_{C1}+\widehat{v_{C1}} \\ V_{C3}+\widehat{v_{C3}} \\ I_{Ldc}+\widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2L} \end{bmatrix} v_{in}$$

▪ Small-Signal Modeling of the Three-Phase Unfolding Inverter

- **D1 reference small signal model**

$$\begin{bmatrix} \frac{d(V_{C1}+\widehat{v_{C1}})}{dt} \\ \frac{d(V_{C3}+\widehat{v_{C3}})}{dt} \\ \frac{d(I_{Ldc}+\widehat{i_{Ldc}})}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1+\widehat{d1}}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ \frac{D4-2*(D1+\widehat{d1})}{2L} & \frac{2*D4-(D1+\widehat{d1})}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_{C1}+\widehat{v_{C1}} \\ V_{C3}+\widehat{v_{C3}} \\ I_{Ldc}+\widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2L} \end{bmatrix} v_{in}$$

- $\frac{d(\widehat{v_{C1}})}{dt} = \left(-\frac{1}{C_1R}\right) * (\widehat{v_{C1}}) + \left(\frac{\widehat{d1}}{C_1}\right) * (I_{Ldc}) + \left(\frac{D1}{C_1}\right) * (\widehat{i_{Ldc}})$
- $\frac{d(\widehat{v_{C3}})}{dt} = \left(-\frac{1}{C_3R}\right) * (\widehat{v_{C3}}) + (-\frac{D4}{C_3}) * (\widehat{i_{Ldc}})$
- $\frac{d(\widehat{i_{Ldc}})}{dt} = \left(-2\frac{\widehat{d1}}{2L}\right) * (V_{C1}) + \left(\frac{D4-2*D1}{2L}\right) * (\widehat{v_{C1}}) + \left(-\frac{\widehat{d1}}{2L}\right) * (V_{C3}) + \left(\frac{2*D4-D1}{2L}\right) * (\widehat{v_{C3}})$

$$\begin{bmatrix} \frac{d\widehat{v_{C1}}}{dt} \\ \frac{d\widehat{v_{C3}}}{dt} \\ \frac{d\widehat{i_{Ldc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ \frac{D4-2*D1}{2L} & \frac{2*D4-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} \widehat{v_{C1}} \\ \widehat{v_{C3}} \\ \widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} \frac{I_{Ldc}}{C_1} \\ 0 \\ -\frac{2V_{C1}+V_{C3}}{2L} \end{bmatrix} \widehat{d1}$$

- **D4 reference small signal model**

$$\begin{bmatrix} \frac{d(V_{C1}+\widehat{v_{C1}})}{dt} \\ \frac{d(V_{C3}+\widehat{v_{C3}})}{dt} \\ \frac{d(I_{Ldc}+\widehat{i_{Ldc}})}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4+\widehat{d4}}{C_3} \\ \frac{D4+\widehat{d4}-2*D1}{2L} & \frac{2*(D4+\widehat{d4})-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_{C1}+\widehat{v_{C1}} \\ V_{C3}+\widehat{v_{C3}} \\ I_{Ldc}+\widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2L} \end{bmatrix} v_{in}$$

- $\frac{d(\widehat{v_{C1}})}{dt} = \left(-\frac{1}{C_1R}\right) * (\widehat{v_{C1}}) + \left(\frac{D1}{C_1}\right) * (\widehat{i_{Ldc}})$
- $\frac{d(\widehat{v_{C3}})}{dt} = \left(-\frac{1}{C_3R}\right) * (\widehat{v_{C3}}) + \left(-\frac{\widehat{d4}}{C_3}\right) * (I_{Ldc}) + (-\frac{D4}{C_3}) * (\widehat{i_{Ldc}})$
- $\frac{d(\widehat{i_{Ldc}})}{dt} = \left(\frac{\widehat{d4}}{2L}\right) * (V_{C1}) + \left(\frac{D4-2*D1}{2L}\right) * (\widehat{v_{C1}}) + \left(2\frac{\widehat{d4}}{2L}\right) * (V_{C3}) + \left(\frac{2*D4-D1}{2L}\right) * (\widehat{v_{C3}})$

$$\begin{bmatrix} \frac{d\widehat{v_{C1}}}{dt} \\ \frac{d\widehat{v_{C3}}}{dt} \\ \frac{d\widehat{i_{Ldc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ \frac{D4-2*D1}{2L} & \frac{2*D4-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} \widehat{v_{C1}} \\ \widehat{v_{C3}} \\ \widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{I_{Ldc}}{C_3} \\ \frac{V_{C1}+2V_{C3}}{2L} \end{bmatrix} \widehat{d4}$$

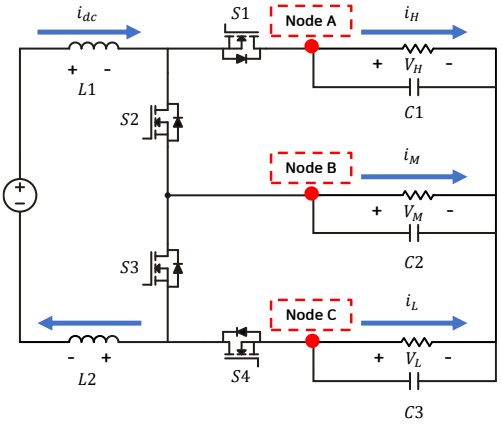
▪ Derivation of the Transfer Function with Respect to D_1

$$\begin{bmatrix} \frac{d\widehat{v_{C1}}}{dt} \\ \frac{d\widehat{v_{C3}}}{dt} \\ \frac{d\widehat{i_{Ldc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ \frac{D4-2*D1}{2L} & \frac{2*D4-D1}{2L} & 0 \end{bmatrix} \begin{bmatrix} \widehat{v_{C1}} \\ \widehat{v_{C3}} \\ \widehat{i_{Ldc}} \end{bmatrix} + \begin{bmatrix} \frac{I_{Ldc}}{C_1} \\ 0 \\ -\frac{2V_{C1}+V_{C3}}{2L} \end{bmatrix} \widehat{d1}, A = \begin{bmatrix} -\frac{1}{C_1R} & 0 & \frac{D1}{C_1} \\ 0 & -\frac{1}{C_3R} & -\frac{D4}{C_3} \\ \frac{D4-2*D1}{2L} & \frac{2*D4-D1}{2L} & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{I_{Ldc}}{C_1} \\ 0 \\ -\frac{2V_{C1}+V_{C3}}{2L} \end{bmatrix}, sI - A = \begin{bmatrix} s+\frac{1}{C_1R} & 0 & -\frac{D1}{C_1} \\ 0 & s+\frac{1}{C_3R} & \frac{D4}{C_3} \\ -\frac{D4-2*D1}{2L} & -\frac{2*D4-D1}{2L} & 0 \end{bmatrix}$$

- $(sI - A)X(s) = BU(s)$ -> Calculate transfer function using Cramer's formula
- $N_{vc1d}(s) = \begin{vmatrix} \frac{I_{Ldc}}{C_1} & 0 & -\frac{D1}{C_1} \\ 0 & s+\frac{1}{C_3R} & \frac{D4}{C_3} \\ -\frac{2V_{C1}+V_{C3}}{2L} & -\frac{2*D4-D1}{2L} & 0 \end{vmatrix} = (\frac{I_L}{C1}) * (s^2 + \frac{s}{C3*R} + \frac{2*D4^2-D1*D4}{2*L*C3}) - (\frac{D1}{C1}) * (\frac{2*V_{C1}+V_{C3}}{2*L}) * (s + \frac{1}{C3*R})$
- $\det(sI - A) = \Delta s = s^3 + \left(\frac{1}{C1*R} + \frac{1}{C3*R}\right) * s^2 + \left(\frac{1}{C1*C3*R^2} - \frac{(D1*D4-2*D1^2)}{2*L*C1} - \frac{(D1*D4-2*D4^2)}{2*L*C3}\right) * s + \frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}$
- $\frac{V_{C1}(s)}{d_1(s)} = \frac{N_{vc1d}(s)}{\Delta s} = \frac{(\frac{I_L}{C1})*(s^2+\frac{s}{C3*R}+\frac{2*D4^2-D1*D4}{2*L*C3})-(\frac{D1}{C1})*(\frac{2*V_{C1}+V_{C3}}{2*L})*(s+\frac{1}{C3*R})}{s^3+\left(\frac{1}{C1*R}+\frac{1}{C3*R}\right)*s^2+\left(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3}\right)*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$

▪ Three Phase Unfolding Inverter overall transfer function

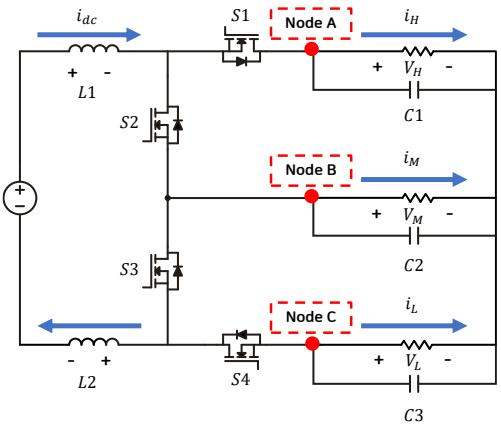
- $\frac{V_{C1}(s)}{d_1(s)} = \frac{\frac{I_L}{C1}*s^2+(\frac{I_{Ldc}}{C1*C3*R}-\frac{D1(2V_{C1}+V_{C3})}{2*C1*L})s+\frac{2D4^2*I_{Ldc}-D1*D4*I_{Ldc}}{2*C1*C3*L}-\frac{2V_{C1}*D1+V_{C3}*D1}{2*C1*C3*L*R}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$
- $\frac{V_{C3}(s)}{d_1(s)} = \frac{\frac{D4(2V_{C1}+V_{C3})}{2*C3*L}*s+\frac{D4(2V_{C1}+V_{C3})}{2*C1*C3*L*R}-\frac{D4*I_{Ldc}(D_4-2D_1)}{2*C1*C3L}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$
- $\frac{V_{C1}(s)}{d_4(s)} = \frac{\frac{D1(V_{C1}+2V_{C3})}{2*C1*L}*s+\frac{D1(V_{C1}+2V_{C3})}{2*C1*C3*L*R}-\frac{D1*I_{Ldc}(2D_4-D_1)}{2*C1*C3L}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$
- $\frac{V_{C3}(s)}{d_4(s)} = \frac{-\frac{I_L}{C3}*s^2+(-\frac{I_{Ldc}}{C1*C3*R}-\frac{D4(V_{C1}+2V_{C3})}{2*C3*L})s+\frac{D1*D4*I_{Ldc}-2D1^2*I_{Ldc}}{2*C1*C3*L}-\frac{V_{C1}*D4+2V_{C3}*D4}{2*C1*C3*L*R}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$
- $\frac{I_{Ldc}(s)}{d_1(s)} = \frac{-(\frac{2V_{C1}+V_{C3}}{2L})*s^2+(\frac{(D4-2D1)I_{Ldc}}{2*C1*L}-\frac{2V_{C1}+V_{C3}}{2L}(\frac{1}{C1R}+\frac{1}{C_3R}))*s+\frac{(D4-2D1)I_{Ldc}}{2*C1*C3*L*R}-\frac{2V_{C1}+V_{C3}}{2*C1*C3*L*R^2}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$
- $\frac{I_{Ldc}(s)}{d_4(s)} = \frac{(\frac{V_{C1}+2V_{C3}}{2L})*s^2+(-\frac{(2D4-D1)I_{Ldc}}{2*C3*L}-\frac{V_{C1}+2V_{C3}}{2L}(\frac{1}{C1R}+\frac{1}{C_3R}))*s-\frac{(2D4-D1)I_{Ldc}}{2*C1*C3*L*R}+\frac{V_{C1}+2V_{C3}}{2*C1*C3*L*R^2}}{s^3+(\frac{1}{C1*R}+\frac{1}{C3*R})*s^2+(\frac{1}{C1*C3*R^2}-\frac{(D1*D4-2*D1^2)}{2*L*C1}-\frac{(D1*D4-2*D4^2)}{2*L*C3})*s+\frac{(D1^2-D1*D4+D4^2)}{C1*C3*R*L}}$



<Simplified equivalent circuit>

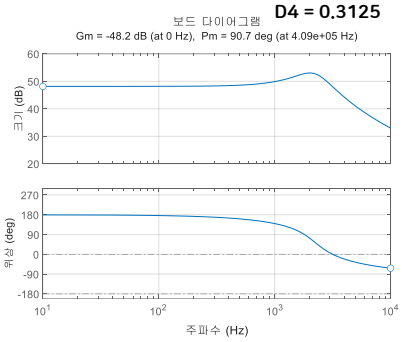
- **A total of six transfer functions are derived.**

▪ Bode plot of the Three Phase Unfolding Inverter



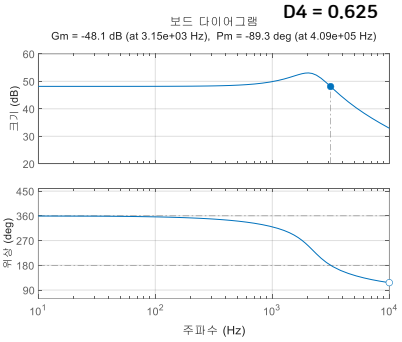
<Simplified equivalent circuit>

D1 =0.625
D4 = 0.3125



<$V_{C1}(s)/d_1(s)$ Bode plot >

D1 = 0.3125
D4 = 0.625

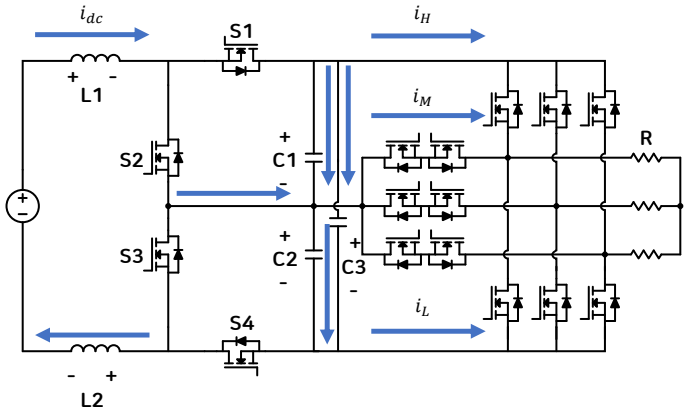


<$V_{C3}(s)/d_4(s)$ Bode plot >

- **Bode plot of the simplified equivalent circuit transfer function via MATLAB**

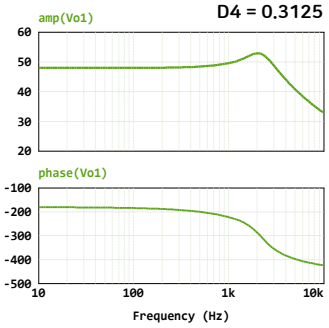
		$\frac{V_{C1}(s)}{d_1(s)}$	$\frac{V_{C3}(s)}{d_4(s)}$
100Hz (Matlab)	magnitude	48dB	48dB
	phase	177°	357°
1kHz (Matlab)	magnitude	49.5dB	49.5dB
	phase	139°	319°

▪ Bode plot of the Three Phase Unfolding Inverter



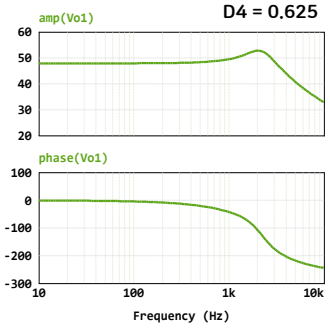
< Three Phase Unfolding Inverter Circuit>

D1 =0.625
D4 = 0.3125



< $V_H(s)$ /$d_1(s)$ Bode plot >

D1 = 0.3125
D4 = 0.625



<$V_L(s)$ /$d_4(s)$ Bode plot >

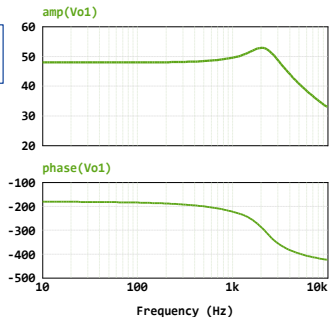
- Bode plot of the TLBC unfolding inverter circuit via PSIM AC Sweep

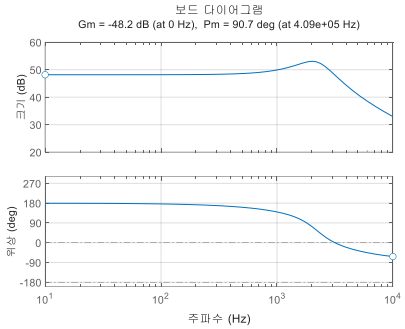
		$\frac{V_{C1}(s)}{d_1(s)}$	$\frac{V_{C3}(s)}{d_4(s)}$
100Hz	magnitude	48dB	48dB
	phase	-183°	-3°
1kHz	magnitude	49.5dB	49.5dB
	phase	-221°	-41°

▪ Comparison of MATLAB and PSIM AC Sweep

$$\frac{V_H(s)}{d_1(s)} = \frac{V_{C1}(s)}{d_1(s)}$$

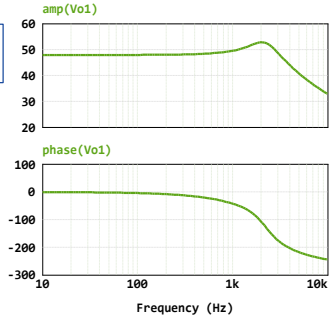
D1 =0.625
D4 = 0.3125

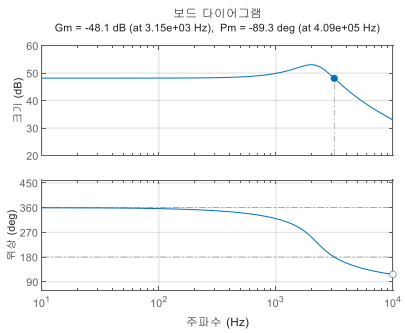




$$\frac{V_L(s)}{d_4(s)} = \frac{V_{C3}(s)}{d_4(s)}$$

D1 = 0.3125
D4 = 0.625





- Comparison of Transfer Function and PSIM AC Sweep
- The magnitude (dB) matches.
- The phase agrees within 360° (i.e., effectively identical).

		$\frac{V_{C1}(s)}{d_1(s)}$	$\frac{V_{C3}(s)}{d_4(s)}$
100Hz (PSIM)	magnitude	48dB	48dB
	phase	-183°	-3°
100Hz (Matlab)	magnitude	48dB	48dB
	phase	177°	357°
1kHz (PSIM)	magnitude	49.5dB	49.5dB
	phase	-221°	-41°
1kHz (Matlab)	magnitude	49.5dB	49.5dB
	phase	139°	319°

Conclusion

① Summary
- Operation analysis of the three-phase unfolding inverter was performed by analyzing 4 switching steps and 2 averaged modes.
- The equivalent circuit was simplified by removing the T-type stage and converting the capacitor bank from delta to wye, enabling tractable analysis.
- Small-signal modeling via state-space averaging yielded six transfer functions with respect to the duty ratios.
- The model was validated against PSIM AC-sweep: magnitude in dB matches and phase matches within a 360° offset.

② Significance
- Previous Research[1] lacks a transfer-function model (only static KCL/KVL relations), and Previous Research[2] requires a dual-converter input stage.
- This work derives the missing MIMO small-signal transfer function on a single-converter input stage (TLBC).
- The derived transfer function makes stability and bandwidth analytically predictable, providing a clear basis for systematic controller design.

③ Future Work
- Closed-loop voltage / current controller design based on the derived MIMO plant.
- Hardware experimental verification with a prototype.

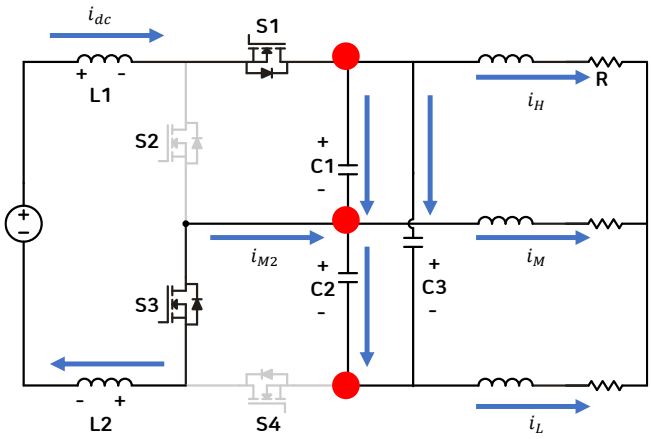
Q & A

Appendix

▪ Three Phase Unfolding Inverter Operation Analysis

PEEC Laboratry

▪ Step1



- $V_M = -V_H - V_L$
- $V_{C1} = V_H - V_M$
- $V_{C2} = V_M - V_L$
- $V_{C3} = V_H - V_L$

→

- $V_M = \frac{V_{C2} - V_{C1}}{3}$
- $V_H = \frac{2V_{C1} + V_{C2}}{3}$
- $V_L = -\frac{V_{C1} + 2V_{C2}}{3}$

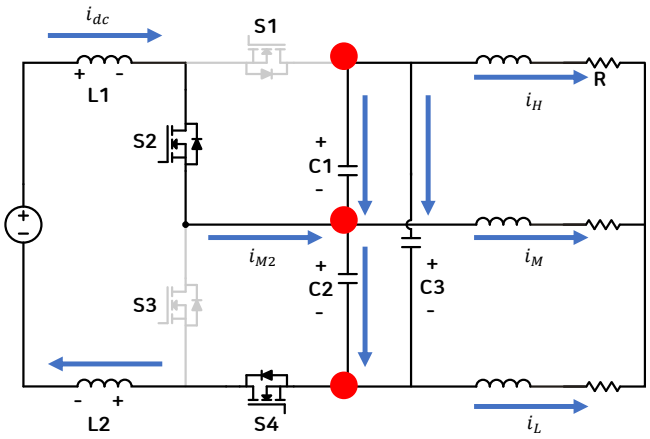
- $i_{C1} + i_{C3} = i_{dc} - i_H$
- $C1\frac{dV_{C1}}{dt} + C3\frac{dV_{C3}}{dt} = i_{dc} - i_H = i_{dc} - \frac{V_H}{R} = i_{dc} - \frac{2V_{C1} + V_{C2}}{3R}$

- $i_{C1} - i_{C2} = i_M - i_{M2}$
- $C1\frac{dV_{C1}}{dt} - C2\frac{dV_{C2}}{dt} = i_M - i_{M2}$

- $i_{C2} + i_{C3} = i_L$
- $C2\frac{dV_{C2}}{dt} + C3\frac{dV_{C3}}{dt} = i_L = \frac{V_L}{R} = -\frac{V_{C1} + 2V_{C2}}{3R}$

- $2V_L = V_{in} - V_{C1}$
- $\frac{di_L}{dt} = \frac{V_{in} - V_{C1}}{2L}$

▪ Step2



- $V_M = -V_H - V_L$
- $V_{C1} = V_H - V_M$
- $V_{C2} = V_M - V_L$
- $V_{C3} = V_H - V_L$

→

- $V_M = \frac{V_{C2} - V_{C1}}{3}$
- $V_H = \frac{2V_{C1} + V_{C2}}{3}$
- $V_L = -\frac{V_{C1} + 2V_{C2}}{3}$

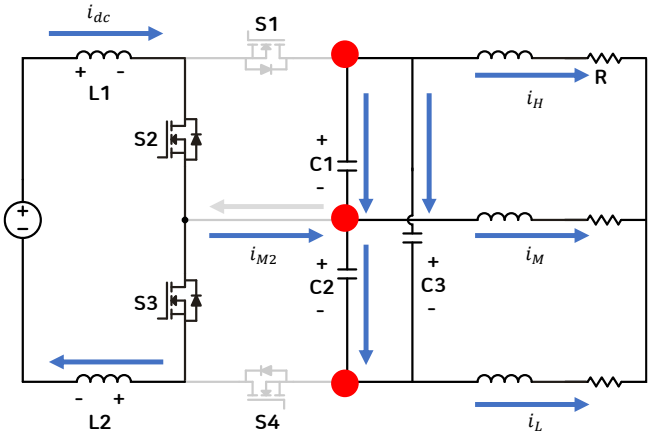
- $i_{C1} + i_{C3} = -i_H$
- $C1\frac{dV_{C1}}{dt} + C3\frac{dV_{C3}}{dt} = -i_H = -\frac{V_H}{R} = -\frac{2V_{C1} + V_{C2}}{3R}$

- $i_{C1} - i_{C2} = i_M - i_{M2}$
- $C1\frac{dV_{C1}}{dt} - C2\frac{dV_{C2}}{dt} = i_M - i_{M2}$

- $i_{C2} + i_{C3} = i_{dc} + i_L$
- $C2\frac{dV_{C2}}{dt} + C3\frac{dV_{C3}}{dt} = i_{dc} + i_L = i_{dc} + \frac{V_L}{R} = i_{dc} - \frac{V_{C1} + 2V_{C2}}{3R}$

- $2V_L = V_{in} - V_{C2}$
- $\frac{di_L}{dt} = \frac{V_{in} - V_{C2}}{2L}$

▪ Step3



- $V_M = -V_H - V_L$
- $V_{C1} = V_H - V_M$
- $V_{C2} = V_M - V_L$
- $V_{C3} = V_H - V_L$

→

- $V_M = \frac{V_{C2} - V_{C1}}{3}$
- $V_H = \frac{2V_{C1} + V_{C2}}{3}$
- $V_L = -\frac{V_{C1} + 2V_{C2}}{3}$

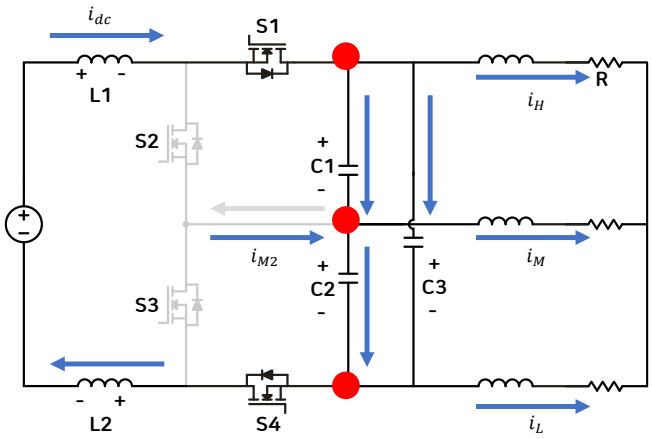
- $i_{C1} + i_{C3} = -i_H$
- $C1\frac{dV_{C1}}{dt} + C3\frac{dV_{C3}}{dt} = -i_H = -\frac{V_H}{R} = -\frac{2V_{C1} + V_{C2}}{3R}$

- $i_{C1} - i_{C2} = i_M$
- $C1\frac{dV_{C1}}{dt} - C2\frac{dV_{C2}}{dt} = i_M$

- $i_{C2} + i_{C3} = i_L$
- $C2\frac{dV_{C2}}{dt} + C3\frac{dV_{C3}}{dt} = i_L = \frac{V_L}{R} = -\frac{V_{C1} + 2V_{C2}}{3R}$

- $2V_L = V_{in}$
- $\frac{di_L}{dt} = \frac{V_{in}}{2L}$

▪ Step4



- $V_M = -V_H - V_L$
- $V_{C1} = V_H - V_M$
- $V_{C2} = V_M - V_L$
- $V_{C3} = V_H - V_L$

→

- $V_M = \frac{V_{C2} - V_{C1}}{3}$
- $V_H = \frac{2V_{C1} + V_{C2}}{3}$
- $V_L = -\frac{V_{C1} + 2V_{C2}}{3}$

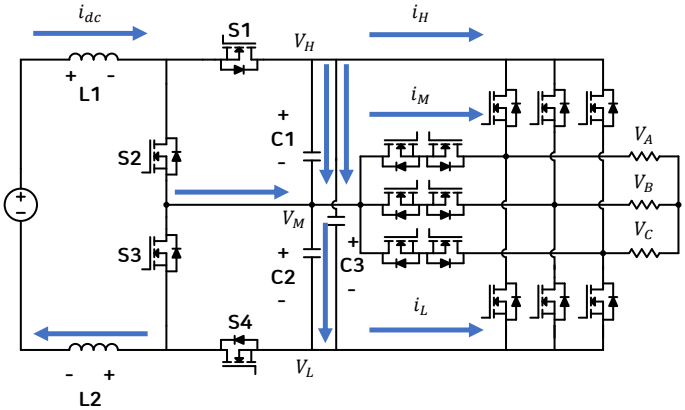
- $i_{C1} + i_{C3} = i_{dc} - i_H$
- $C1\frac{dV_{C1}}{dt} + C3\frac{dV_{C3}}{dt} = i_{dc} - i_H = i_{dc} - \frac{V_H}{R} = i_{dc} - \frac{2V_{C1} + V_{C2}}{3R}$

- $i_{C1} - i_{C2} = i_M$
- $C1\frac{dV_{C1}}{dt} - C2\frac{dV_{C2}}{dt} = i_M$

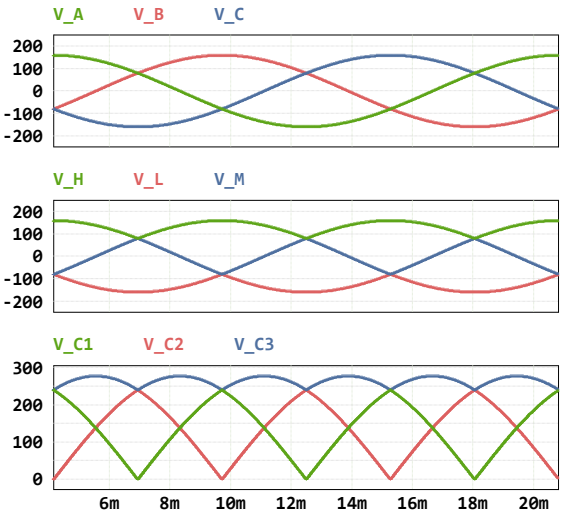
- $i_{C2} + i_{C3} = i_{dc} + i_L$
- $C2\frac{dV_{C2}}{dt} + C3\frac{dV_{C3}}{dt} = i_{dc} + i_L = i_{dc} + \frac{V_L}{R} = i_{dc} - \frac{V_{C1} + 2V_{C2}}{3R}$

- $2V_L = V_{in} - V_{C3} = V_{in} - V_H + V_L$
- $\frac{di_L}{dt} = \frac{V_{in}}{2L} - \frac{2V_{C1} + V_{C2}}{6L} - \frac{V_{C1} + 2V_{C2}}{6L}$

▪ Key operating waveforms of the Three Phase Unfolding Inverter



< Three Phase Unfolding Inverter Circuit>



<Key operating waveforms>

- Key operating waveforms of the three-phase unfolding inverter.
- Each capacitor voltage is shaped by the TLBC converter, and the three-phase unfolding circuit alternates its polarity to generate the three-phase AC output.

Fundamental Study on Density-Based Topology Optimization Methods in Electromagnetic Fields

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2026/05/14 JUSW2026

Outline

- Density-Based Topology Optimization Methods
- Background
- Purpose
- Propose Methods
- Analysis Model
- Consideration
- Conclusion

Density-Based Topology Optimization Methods

Topology optimization methods is widely used in the field of design on electromagnetic devices.

$\rho^{k+1} = \rho^k + \Delta\rho^k$ **ρ : density**

$$\mu = \mu_0\{1 + (\mu_r - 1)\rho^n\}$$

Background

Density-based topology optimization has the following issues:

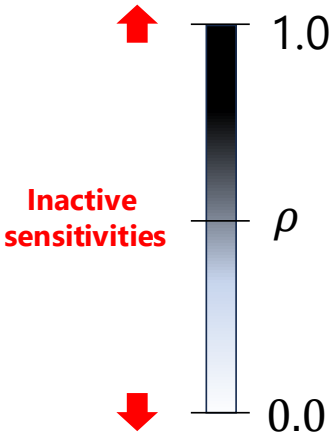
･Inactive sensitivities at density bounds (ρ = 0 or 1)
･Vanishing sensitivity in low-density regions

These problems degrade convergence and solution quality

①*Inactive sensitivities at density bounds*

Sensitivity may suggest decreasing density at ρ = 0 or increasing density at ρ = 1

→ Inactive sensitivity updates
→ Causes slow convergence



②*Vanishing sensitivity in low-density regions*

Permeability interpolation:

$$\mu = \mu_0\{1 + (\mu_r - 1)\rho^n\}$$

$$\frac{\partial \mu}{\partial \rho} \propto n\rho^{n-1}$$

→ Gradient vanishes as ρ → 0
→ Design variables fail to update
→ Optimization stagnates

Purpose

To improve both:

・Update quality (Eliminating unnecessary updates)
・Update quantity (Ensuring gradient availability)

→ Achieve effective design variable updates

Propose Methods

For Problem 1
Sensitivity Enhancement : Method(a)
For Problem 2
Avoidance of zero sensitivity (Introduction of ρ_{min})
: Method(b)

→ Simultaneous control of update quality and quantity

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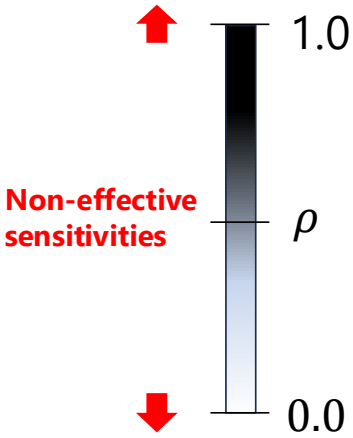
The Method (a) : *Sensitivity Enhancement*

Conditional sensitivity:

ρ = 0 and ∂W/∂ρ > 0 → set to 0
ρ = 1 and ∂W/∂ρ < 0 → set to 0

→ Removes unphysical updates



Effects:
・Improving convergence stability
・Eliminating unnecessary updates

The Method (b) : *Avoidance of Zero Sensitivity*

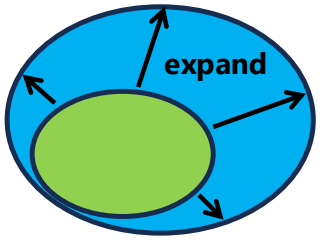
Introduce minimum density ρ_{min}

$$\mu(\rho) = \frac{(1-\rho^n)\mu_{air} + (\rho^n - {\rho_{min}}^n)\rho_{iron}}{1 - {\rho_{min}}^n}$$

$$\mu(\rho_{min}) = \mu_{air}$$
$$\mu(1.0) = \mu_{iron}$$

→ Restrict: $\rho \geq \rho_{min}$

Effects:
・Preventing zero gradient
・Ensuring updates of design variables



Search domain for the solution

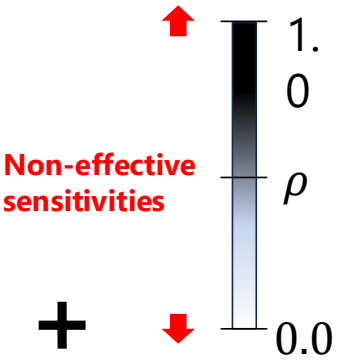
Integration of Methods

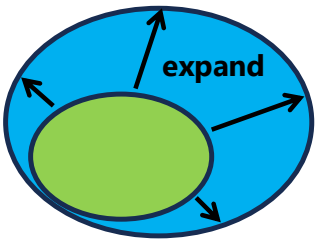
method(a): eliminates unnecessary updates
method(b): ensures necessary updates

(a) only:
→ update becomes insufficient

(b) only:
→ noisy updates remain

(a) + (b):
→ stable and continuous update



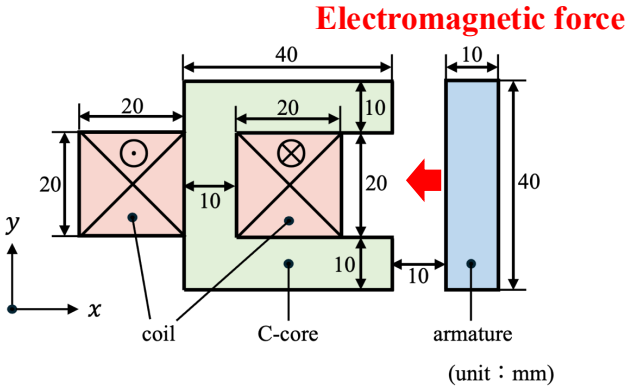


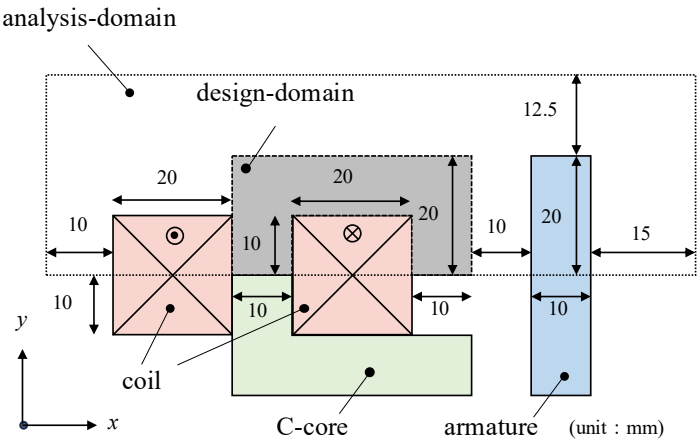
Search domain for the solution

Analysis Model (1)

To verify the effectiveness of the proposed methods, we apply them to the following model:

2D C-core model : Objective : Minimize electromagnetic force





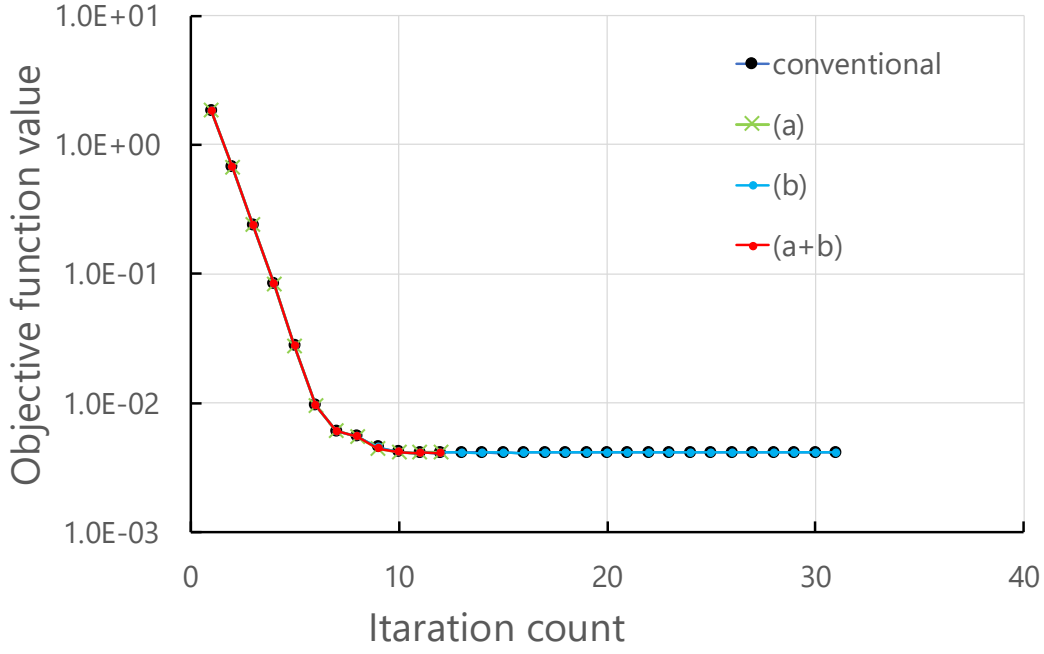
Analysis specifications

Analysis specifications

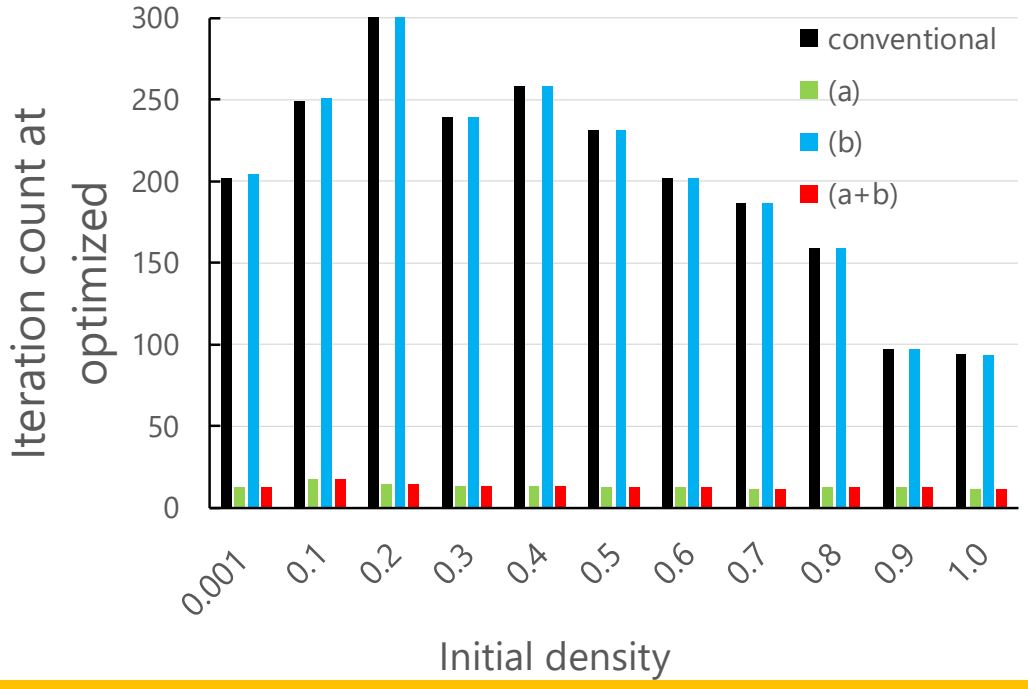
Number of elements	13,650
Number of nodes	13,926
Number of elements in design domain	2,400
Current density	2.0e6
Relative permeability of armature	1,000

- Bilinear quadrilateral elements
- Fortran implementation
- ICCG Method
  Convergence criterion : 10^{-12}

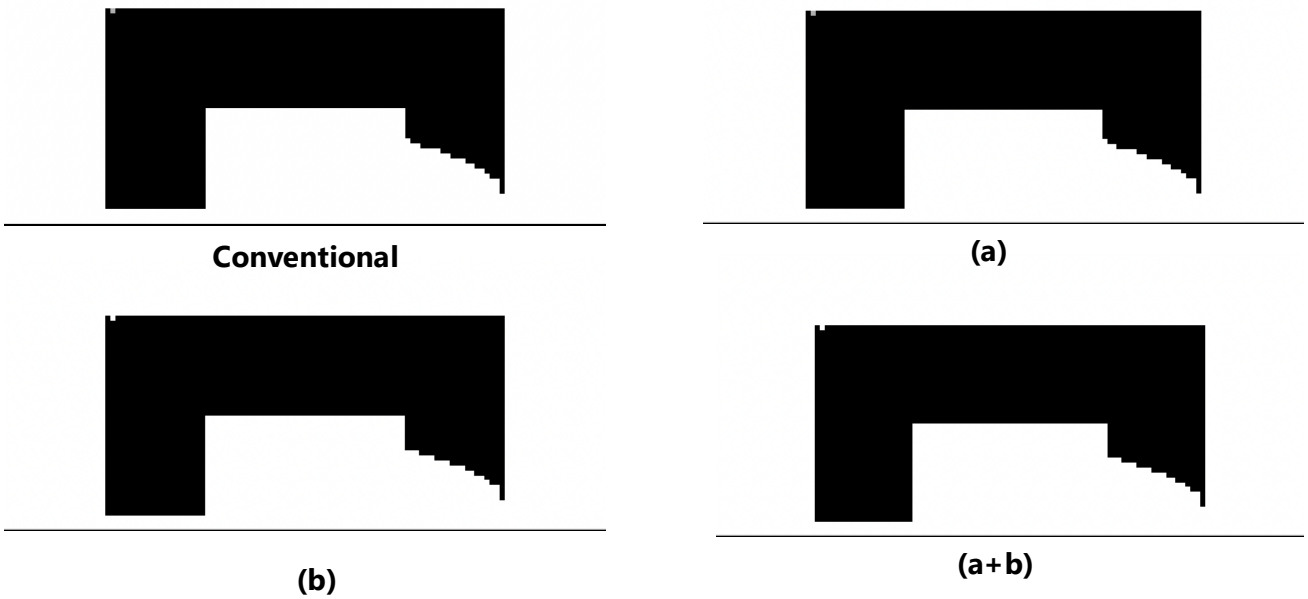
Result : Objective value



Result : *Number of Iterations*



Result : Optimized Shape



Conclusion

・Two issues in density-based update are identified
・Corresponding methods are proposed

→ Both update quality and quantity are improved
→ Optimization performance is enhanced

Thank you for listening.

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