

# Analysis of Gate Drive Circuit for GaN HEMT

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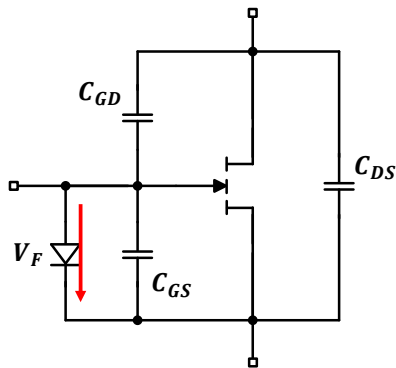
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# 1. Introduction

## Gate Injection Transistor (GIT) GaN

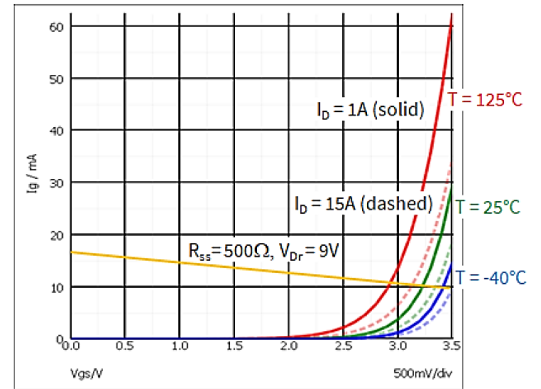
- non-isolated gate structure with a gate diode
- provides a very reliable and robust gate structure
- have a low threshold voltage ( $V_{th}$ )



$R_{ss}$  : stegate resistanceeady-state

$V_{dr}$  : Gate driving voltage

$V_f$  : Gate diode forward voltage



- Gate Diode Conduction Characteristic

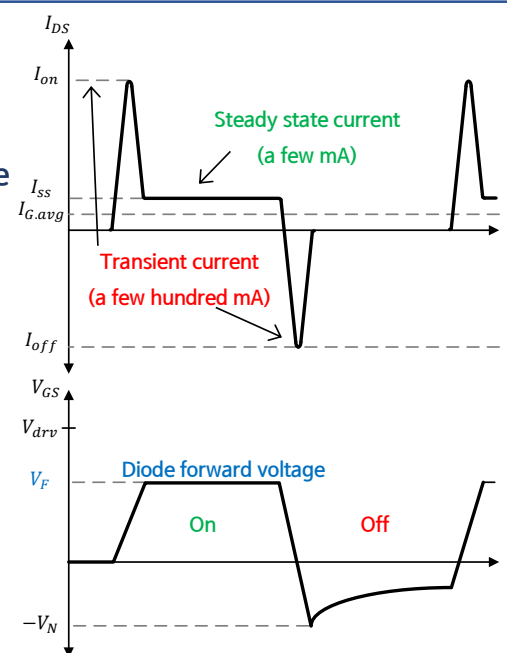
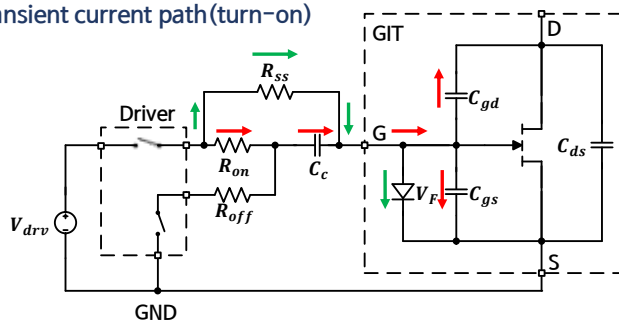
# 2. Gate driving circuit analysis

## RC interface gate driving circuit

- Steady-state current and transient current can be separated
- Reverse voltage can be supplied by a single power source due to the charge accumulated in  $C_c$ .

→ Steady-state current path

→ Transient current path (turn-on)



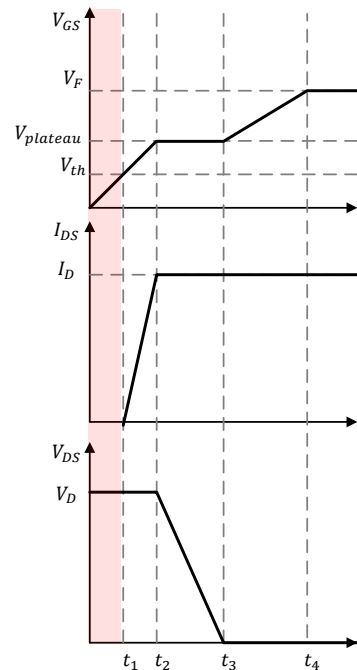
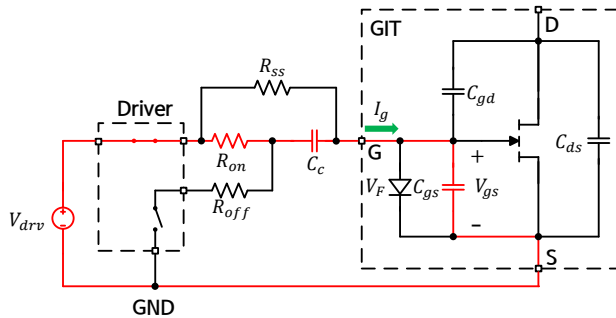
## 2. Gate driving circuit analysis

- Turn-on delay region ( $\sim t_1$ ) Assume,  $R_{ss} \gg R_{on}, C_s \gg C_{GS}$

$$v_{GS} = V_{th} \cdot \left(1 - e^{-\frac{t}{t_f}}\right) \quad t_f \approx R_{on} C_{GS}$$

$$i_G = I_{G0} \cdot e^{-\frac{t}{t_f}}$$

$$t_1 \approx R_{on} C_{GS} \cdot \ln\left(\frac{v_G}{v_G - V_{th}}\right)$$



## 2. Gate driving circuit analysis

- Current increases region ( $t_1 \sim t_2$ ) Assume,  $R_{ss} \gg R_{on}, C_s \gg C_{GS}$

$$i_G = I_{G1} \cdot e^{-\frac{t-t_1}{t_f}}$$

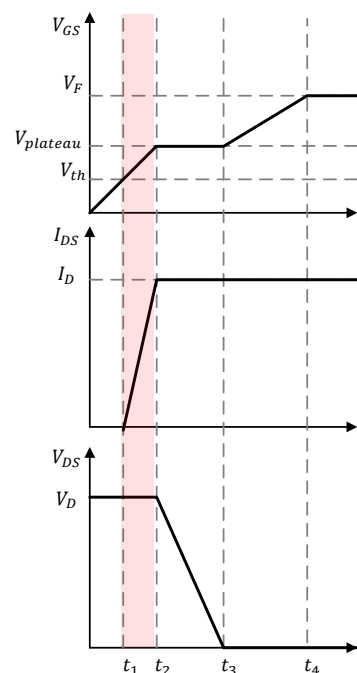
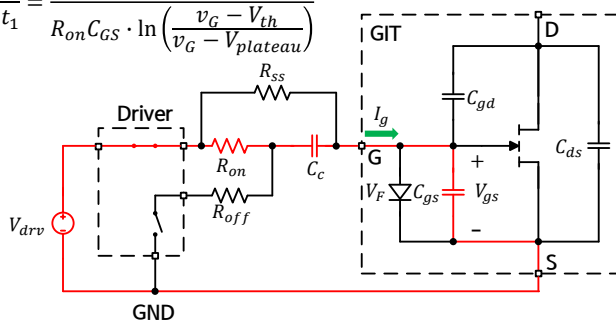
$$t_f \approx R_{on} C_{GS}$$

$$I_{G1} = I_{G0} \cdot e^{-\frac{t}{t_f}}$$

$$t_2 - t_1 \approx R_{on} C_{GS} \cdot \ln\left(\frac{v_G - V_{th}}{v_G - V_{plateau}}\right)$$



$$\frac{di_D}{dt} \approx \frac{I_L}{t_2 - t_1} = \frac{I_L}{R_{on} C_{GS} \cdot \ln\left(\frac{v_G - V_{th}}{v_G - V_{plateau}}\right)}$$

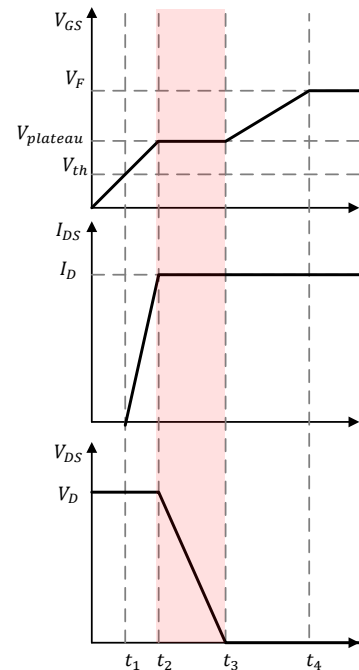
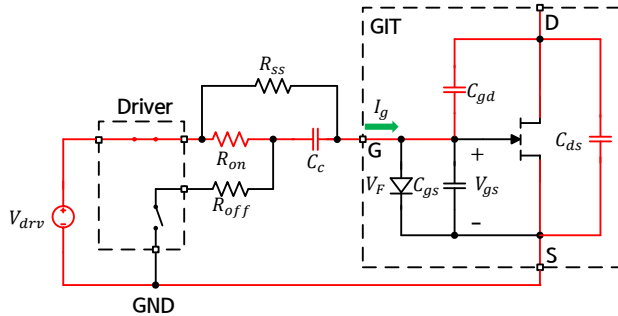


## 2. Gate driving circuit analysis

### Voltage fall region ( $t_2 \sim t_3$ )

Assume,  $R_{ss} \gg R_{on}, C_s \gg C_{GS}$

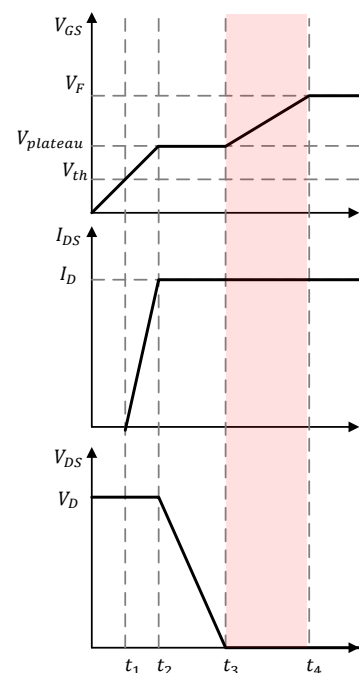
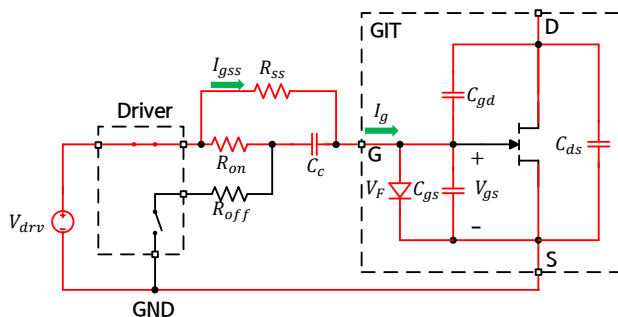
- $v_{GS} = V_{plateau}$
- $i_G \approx \frac{V_G - V_{plateau}}{R_{on}} = -C_{GD} \frac{dv_{DS}}{dt} \Rightarrow \frac{dv_{DS}}{dt} \approx -\frac{V_G - V_{plateau}}{R_{on} C_{GD}}$
- $t_3 - t_2 \approx \frac{R_{on} C_{GD} V_{DC}}{V_G - V_{plateau}}$



## 2. Gate driving circuit analysis

### Enhance the conducting channel region ( $t_3 \sim t_4$ )

- $v_{GS} = V_D - (V_G - V_{plateau}) \cdot e^{-\frac{t-t_3}{\tau_s}}$        $\tau_f \approx R_{on} C_{GD}$        $i_{GSS} = \frac{V_G - V_D}{R_{ss}}$
- $i_G = I_{GSS} + \frac{V_G - V_{plateau}}{R_{on}} \cdot e^{-\frac{t-t_3}{\tau_s}}$



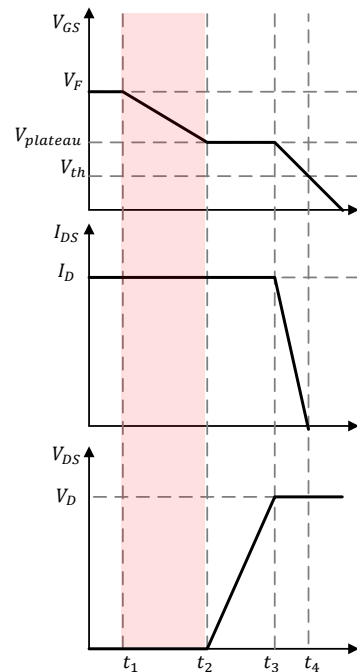
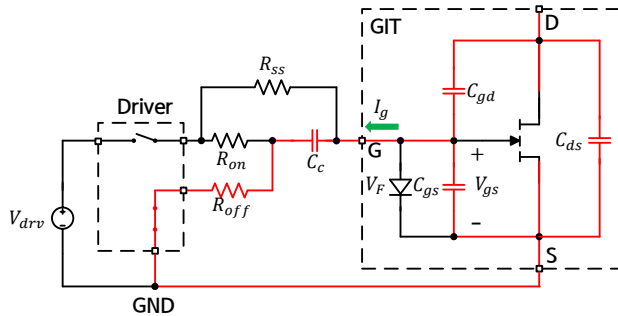
## 2. Gate driving circuit analysis

### ▪ Turn-off delay region ( $t_1 \sim t_2$ )

$$v_{GS} = V_D \cdot e^{-\frac{t}{t_{off}}}$$

$$t_{off} \approx R_{off} C_{GS}$$

$$i_G = \frac{V_G - V_D}{R_{off}} + \frac{V_D}{R_{off}} \cdot e^{-\frac{t}{t_{off}}} + C_{GD} \frac{dv_{GS}}{dt}$$



## 2. Gate driving circuit analysis

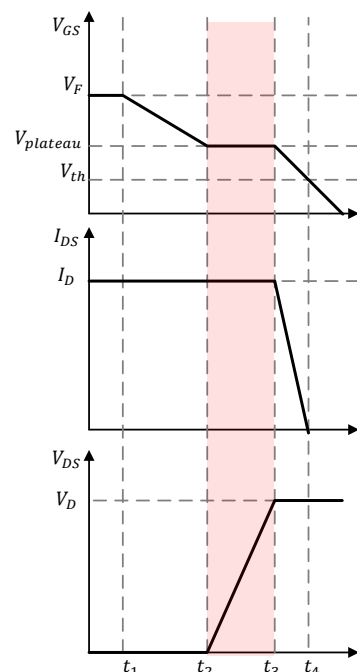
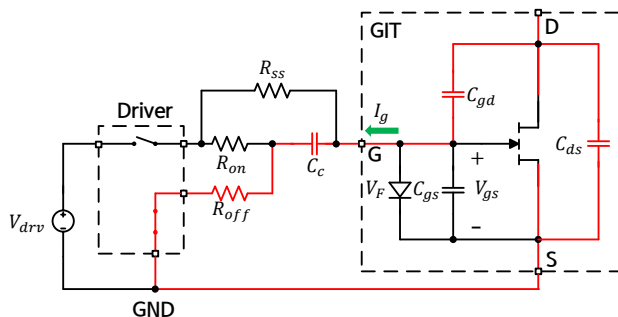
### ▪ Voltage increases region ( $t_2 \sim t_3$ )

$$v_{GS} = V_{plateau}$$

$$t_{off} \approx R_{off} C_{GS}$$

$$i_G = C_{GD} \frac{dv_{DS}}{dt} = \frac{V_G - V_D + V_{plateau}}{R_{off}} \Rightarrow \frac{dv_{DS}}{dt} \approx -\frac{V_G - V_D + V_{plateau}}{R_{off} C_{GD}}$$

$$t_3 - t_2 \approx \frac{R_{on} C_{GD} V_D}{V_G - V_{plateau}}$$



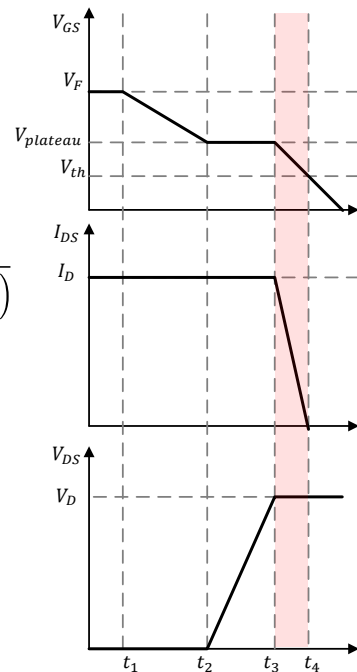
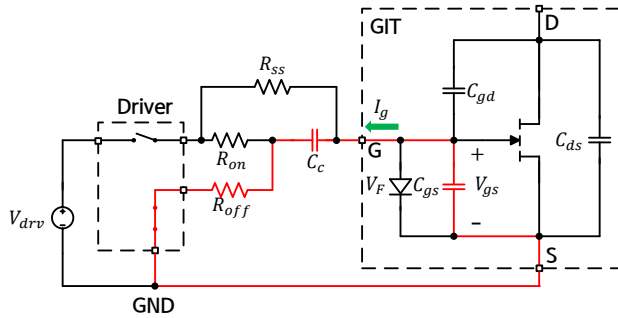
## 2. Gate driving circuit analysis

### ▪ Current fall region ( $t_3 \sim t_4$ )

$$v_{GS} = V_{plateau} \cdot e^{-\frac{t-t_3}{t_{off}}}$$

$$t_{off} \approx R_{off} C_{GS}$$

$$i_G = \frac{V_G - V_D}{R_{off}} + \frac{V_{plateau}}{R_{off}} \cdot e^{-\frac{t-t_3}{t_{off}}} \quad \Rightarrow \quad \frac{di_D}{dt} \approx \frac{I_L}{t_4 - t_3} = \frac{I_L}{R_{off} C_{GS} \cdot \ln\left(\frac{V_{plateau}}{V_{th}}\right)}$$

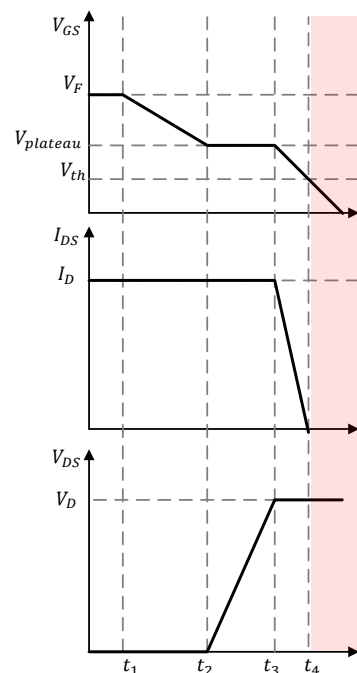
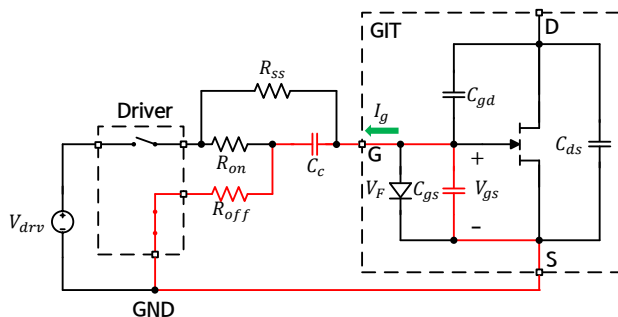


## 2. Gate driving circuit analysis

### ▪ Final gate discharge region ( $\sim t_4$ )

$$v_{GS} = V_{th} \cdot e^{-\frac{t-t_4}{t_{off}}}$$

$$i_G = \frac{V_G - V_D}{R_{off}} + \frac{V_{th}}{R_{off}} \cdot e^{-\frac{t-t_4}{t_{off}}}$$



## 2. Gate driving circuit analysis

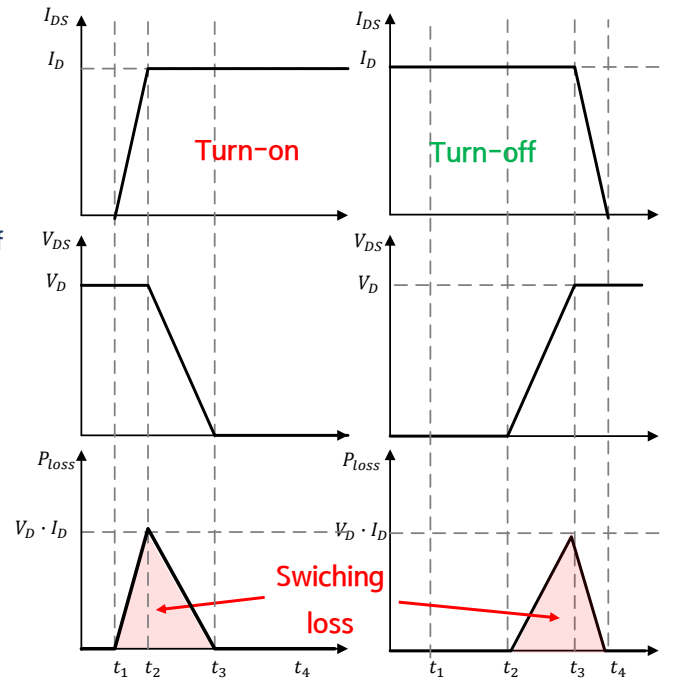
### Switching loss analysis

- $P_{sw} = f_{sw}(E_{on} + E_{off})$ 

$P_{sw}$  : Average switching loss  
 $f_{sw}$  : Switching frequency  
 $E_{on}$  : Energy loss per turn-on  
 $E_{off}$  : Energy loss per turn-off
- $E_{on} = \frac{1}{2} V_D I_D (t_3 - t_1)$ 

$$= \frac{1}{2} V_D I_D R_{on} (C_{GS} \cdot \ln\left(\frac{V_{drv} - V_{th}}{V_{drv} - V_{plateau}}\right) + \frac{C_{GD} V_D}{V_{drv} - V_{plateau}})$$
- $E_{off} = \frac{1}{2} V_D I_D (t_4 - t_2)$ 

$$= \frac{1}{2} V_D I_D R_{off} (C_{GS} \cdot \ln\left(\frac{V_{th}}{V_{plateau}}\right) + \frac{C_{GD} V_D}{V_{drv} - V_F + V_{plateau}})$$



## 2. Gate driving circuit analysis

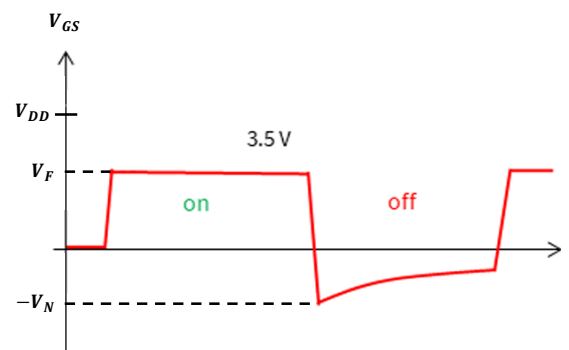
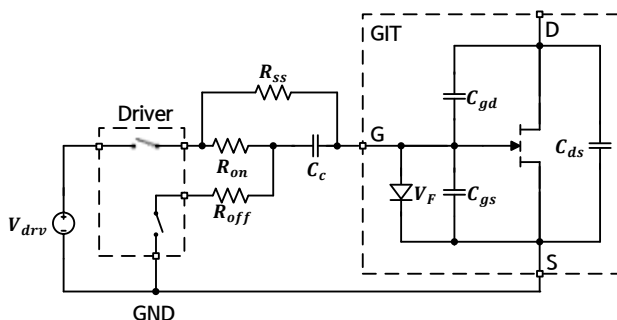
### Design of Cc

- It must be designed to sufficiently discharge the gate charge and generate a negative voltage.

$$-V_N = -\frac{C_c \cdot (V_{drv} - V_F) - Q_G}{C_c + C_{gs}} \quad \Rightarrow \quad C_c > \frac{Q_G}{V_{drv} - V_F}$$

$Q_G$  : Gate charge

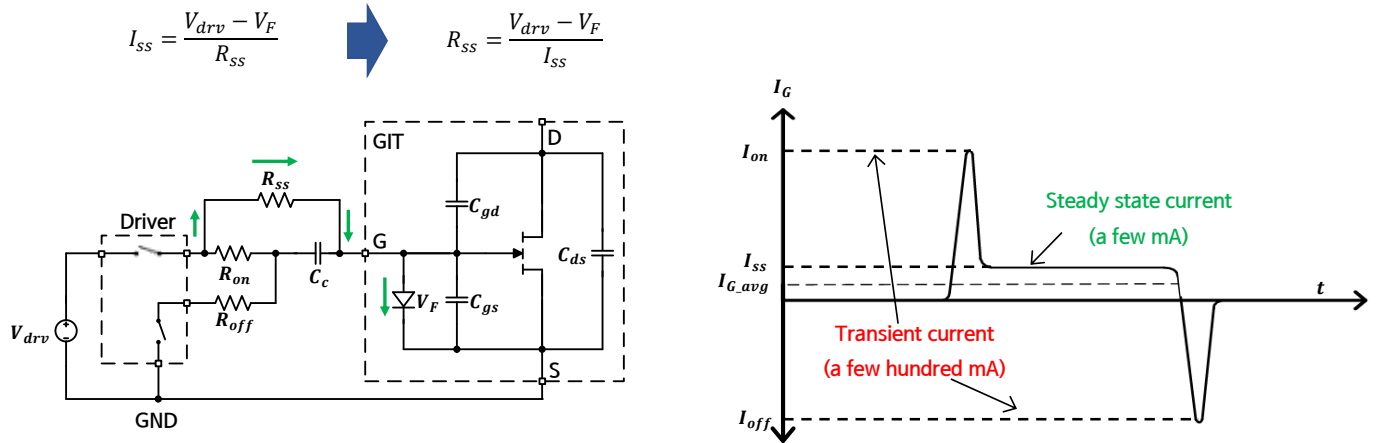
$V_F$  : Gate diode forward voltage



## 2. Gate driving circuit analysis

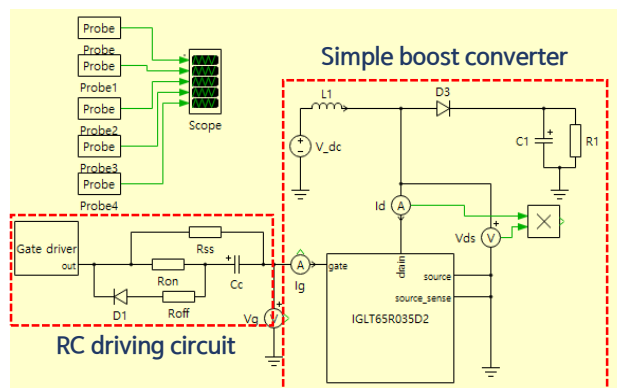
- Design of  $R_{ss}$

- Determined according to steady-state current ( $I_{ss}$ )
- A steady-state current of typically 19 mA is recommended for the 35 mΩ GIT



## 3. Simulation verification

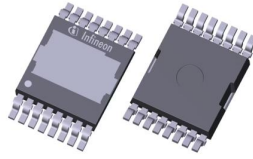
- Simulation verification using PLECS
  - Assuming a gate driver for a 1kW boost converter



Power	1kW	Switching frequency	100kHz
Input voltage	311V	Output voltage	400V

### 3. Simulation verification

- GaN devices used (IGLT65R035D2)



GaN device parameters (Refer to datasheet)

Input capacitance( $C_{iss}$ )	540pF	Output Capacitance( $C_{oss}$ )	91pF
Reverse transfer capacitance( $C_{rss}$ )	13pF	Gate charge( $Q_g$ )	7.7nC
Gate threshold voltage( $V_{th}$ )	1.2V	Maximum drain source voltage	650V
Maximum drain-source voltage slew-rate( $dV/dt$ )	200V/ns	Maximum pulsed drain source current ( $I_{d,pulse}$ )	97A

$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{oss} = C_{ds} + C_{gd}$$

$$C_{rss} = C_{gd}$$

❖ parasitic inductance  
Assuming 10nH



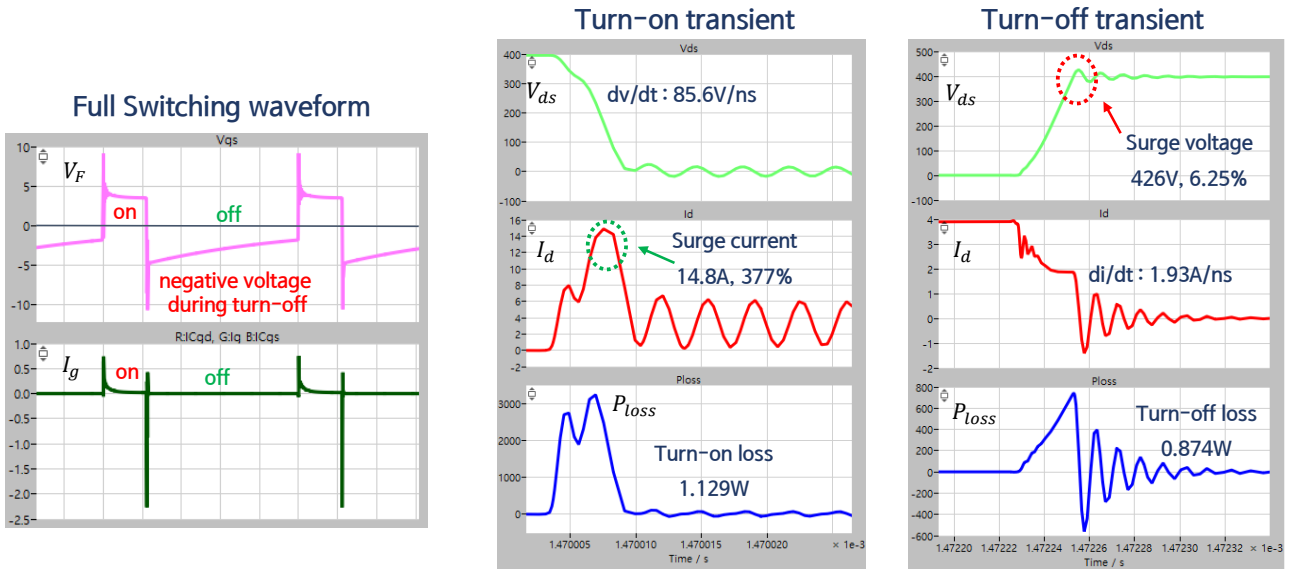
### 3. Simulation verification

- Gate driver parameters in simulation
  - Ron : 12Ω (Determined according to surge current limit)
  - Roff : 1Ω (Determined according to surge voltage limit)
  - Cc : 22nF (Determined to a value that can sufficiently supply a negative voltage)
  - Rss : 340Ω (Determined by the required steady-state current( $I_{ss}$ ))



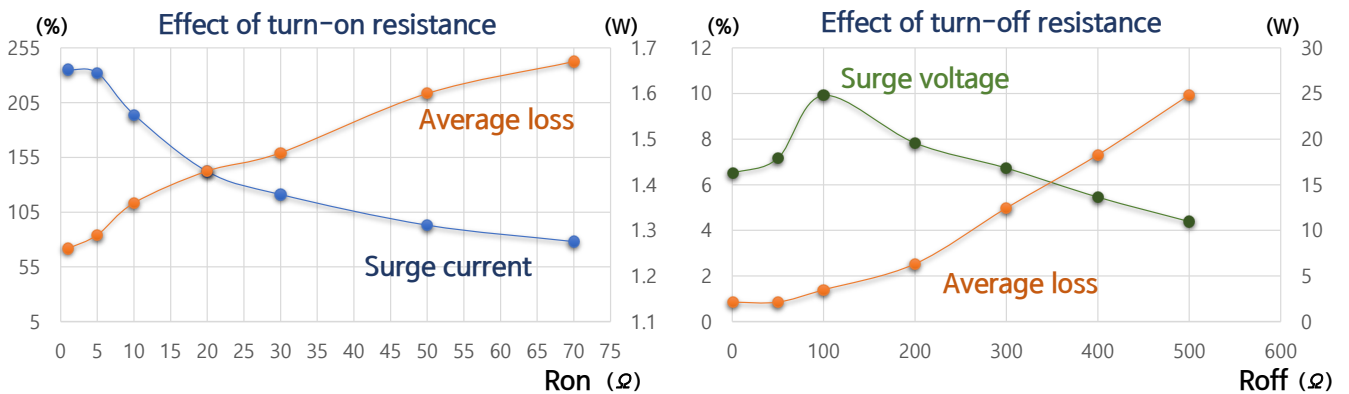
### 3. Simulation verification

- Simulation verification using PLECS



### 3. Simulation verification

- Simulation verification using PLECS



## 4. Conclusion

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- Analysis of gate driver circuits used in GIT
  - Mathematical equations were derived through equivalent circuit analysis of the switching operation.
  - Design guidelines for key parameters were established using the derived equations.
- Simulation Verification
  - The validity of the analytical model was verified through simulation results.
- Expected Impact
  - The proposed approach enables efficient and reliable gate driver design for high-speed switching applications.



Q & A